5VT2528
DATASHEET

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REVISION HISTORY

Revision	Release Date	Author	Change	Remark
V1.0	2021/12/30	Wingston	Initial version	
V1.1	2022/6/1	Wingston	Modify GPIO description, correct 64 GPIO description errors	
V1.2	2022/8/19	Wingston	English version	
	2022/9/22	Wingston	Update BALLMAP,Modify PIN default NAME and Description	
	2022/12/06	Wingston	Fixed the pin location error	
	2022/12/13	Wingston	Add Absolute maximum rating	
	2023/2/6	Wingston	Modify the Serdes IO direction and description	

1 General Description

1.1 Chip Introduction

5VT2528 is an optical modem + switching chip with built-in dual-core 1GHz processor, supporting GPON/EPON/XGPON/XEPON and XGSPON fiber access, as well as Layer 2 switching and Layer 3/4 hardware NAT/NAPT functions as a SOC chip; Equipped with 4 Ethernet ports + 1 RGMII/SGMII/HSGMII + 1 XFI, supports DDR3/DDR4 particles, supports plug-in WIFI chip through PCIE interface to achieve WIFI access, realizing the function of low-cost home optical modem and gateway in one. The chip supports Layer 2 and Layer 3 NAT/NAPT hardwired network switching, and supports WIFI-OFFLOAD hardware acceleration. The chip can be used for a variety of service applications on the upper layer of the processor, such as DHCP, HTTP and some services that require the use of hardwired forwarding functions.

The chip has an integrated GPON/EPON/XGPON/XEPON/XGSPON engine to support network bridging and routing services for handling ultra-low cost optical network terminals.The chip has built-in powerful protocol analysis functions and can handle various hard forwarding services such as VLAN, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP messages. For VLAN and PPPoE protocols, the chip supports automatic encapsulation and decapsulation of VLAN tagged frames and PPPoE headers. The chip supports port-based, protocol-based, VLAN-based, etc. It supports up to 4,000 VLAN groups and supports the SPAN tree protocol, whose states can be divided into four: forbidden, blocking, listening and forwarding.

Features

- System Processor
  1GHz Dual Core Processor
  I-Cache: 32KB
  D-Cache: 32KB
  L2 Cache: 512KB
- Flash Interface
  SPI NAND Flash, SPI NOR Flash, Maximum capacity 32Gb
  Parallel NAND flash, Maximum capacity 32Gb
- Supports 4-ports GEPHY
- Supports DDR3/DDR4
  32-bits DDR3/DDR4
  Supports the highest rate of 2133Mbps
  Maximum capacity 8Gb (1GB)
- 1 USB2.0 interface, Host/Device mode
- 1 USB3.0 interface, Host/Device mode
- 2 PCIE2.0 interfaces, RC mode
- 1 TDM interface, supports TDM+SPI mode
  2 VoIP interface

- 1 ISI interface, 2 VoIP interface
- I2C interface

  Supports 2 I2C interface, 7bit/10bit address mode
- UART interface

  Supports compatible 16550 UART interface

  3 UART interfaces, 1 of which can be multiplexed
- 1 SPI interface
- 1 MDIO interface
- 1 RGMII interface
- Supports 32 GPIO
- GPON

  Compliant with ITU-T G.984.x protocol standard

  Supports data rates of 1.24416G upstream/2.48832G downstream

  Supports 40 TCONT, 320 GEM

  AES128 decryption function

  Support for G.984-required uplink and downlink FEC codecs

  Supports GEM sharding and reorganization

  Supports DBRu reporting

  PLOAM and CRC check

  OMCI processing and CRC check

  Hardware dying gasp

  TYPEB fast switching

  Supports rogue ONU detection

  Supports low power consumption functions required by G.984

  Supports 16384-byte jumbo frames

- XGPON

  Compliant with ITU G.987.x protocol standard

  Supports data rates of 2.48832G upstream/9.95328G downstream

  Supports 40 TCONT, 320 GEM

  Supports AES128 encryption and decryption as required by G.987

  Support for G.987-required uplink and downlink FEC codecs

  Supports DBRu reporting

  Supports G.987 compliant uplink and downlink PLOAM and MIC checksum

  Supports G.988 compliant uplink and downlink OMCI processing and MIC checksum, supports variable length OMCI messages

  Hardware dying gasp

  TYPEB fast switching

  Supports rogue ONU detection

  Supports low power consumption functions required by G.987

  Supports 16384-byte jumbo frames

- XGSPON

  Compliant with ITU G.9807.x protocol standard

Supports data rates of 9.95328G upstream/9.95328G downstream

Supports 40 TCONT, 320 GEM

Supports AES128 encryption and decryption as required by G.9807

Supports for G.9807-required uplink and downlink FEC codecs

Supports DBRu reporting

Supports G.9807 compliant uplink and downlink PLOAM and MIC checksum

Supports G.988 compliant uplink and downlink OMCI processing and MIC checksum, supports variable length OMCI messages

Hardware dying gasp

TYPEB fast switching

Supports rogue ONU detection

Supports low power consumption functions required by G.987

Supports 16384-byte jumbo frames

- EPON

Compliant with IEEE 802.3 EPON MAC standard and CTC EPON equipment technical requirements

8 independent LLIDs, 8 queues per LLID

LLID listening function, support broadcast LLID configurable

Supports data rates of 1.25G upstream/1.25G downstream

Supports bidirectional FEC codec function

Supports triple churning decryption of downlink CTC and AES128 decryption of DPOE standard

Supports multiple queue sets and queue reporting functions

Supports dying gasp

TYPEB fast switching

Supports rogue ONU detection

- XEPON

Compliant with IEEE 802.3 EPON MAC standard and CTC EPON equipment technical requirements

32 independent LLIDs, 8 queues per LLID

LLID listening function, support broadcast LLID configurable

Supports symmetric and asymmetric rate modes: Uplink 1.25G/Downlink 10.3125G or Uplink 10.3125G/Downlink 10.3125G

Supports bidirectional FEC codec function

Supports triple churning decryption of downlink CTC and AES128 decryption of DPOE standard

Supports multiple queue sets and queue reporting functions

Supports dying gasp

TYPEB fast switching

Supports rogue ONU detection

Supports 9600-byte jumbo frames

- US scheduling

(CIR/PIR) Supports queue rate control setting (CIR/PIR)

Supports strict priority and weighted fair queuing modes

Supports RC4837 Counter

Hardware dying gasp

- Layer 2/Layer 3 packet hardware accelerator for NAT/NAPT

Supports 32K NAPT rules /4K NAPTR rules

Supports based on port/VLAN binding

Supports IPv4/IPv6 protocols

Supports IPoE/DHCP/PPPoE/DS-Lite WAN hardware packet accelerator

Supports DS-Lite multicast

Supports VxLAN hardware forwarding

Supports NAPTv6 hardware forwarding

- L2 capability

Supports 4 Gigabit Ethernet ports

Supports non-blocking wire-speed receiving and sending and non-head-of-line blocking/forwarding

Embedded 512 entry 4-way hash L2 lookup table

Supports source and destination MAC address filtering

- Supports ACL

Based on MAC, IP, TCP/UDP, ICMP,IGMP, IPv6

Supports actions of mirror, redirect, dropping

Supports queuing and scheduling, traffic monitoring

CVLAN decision, SVLAN designation

Supports packet length/VID/IP/L4 Port range check

- 16 PON classification rules

Supports SVLAN tagging/removing

Supports CVLAN tagging/removing

Supports indirect LLID/GEMPort specification

Supports forced UNI port forwarding and queue priority designation

- IEEE 802.1Q VLAN

Supports 4K VLAN

Supports Untag definition in each VLAN

Supports VLAN based on port and protocol

- Supports IEEE 802.1ad Stacking VLAN
- Supports 2 users to define TPID
- Supports IVL, SVL, and IVL/SVL
- Supports 512 MAC address table, 4 hash calculation
- Supports spanning Tree
- Supports IEEE 802.3x full-duplex and half-duplex flow control mechanism
- Supports IEEE 802.1X access control protocol
- Supports Quality of Service (QoS)
- Supports strict priority and weighted fair queuing modes
- Supports port to monitoring destination port
- Supports OAM
- Supports IGMP/MLD trap detection function
- Supports to prevent DOS attack

- Supports 1PPS+ToD
- Supports Ethernet SyncE

1.2 Block Diagram

The connection relationship of the chip in the application as below:

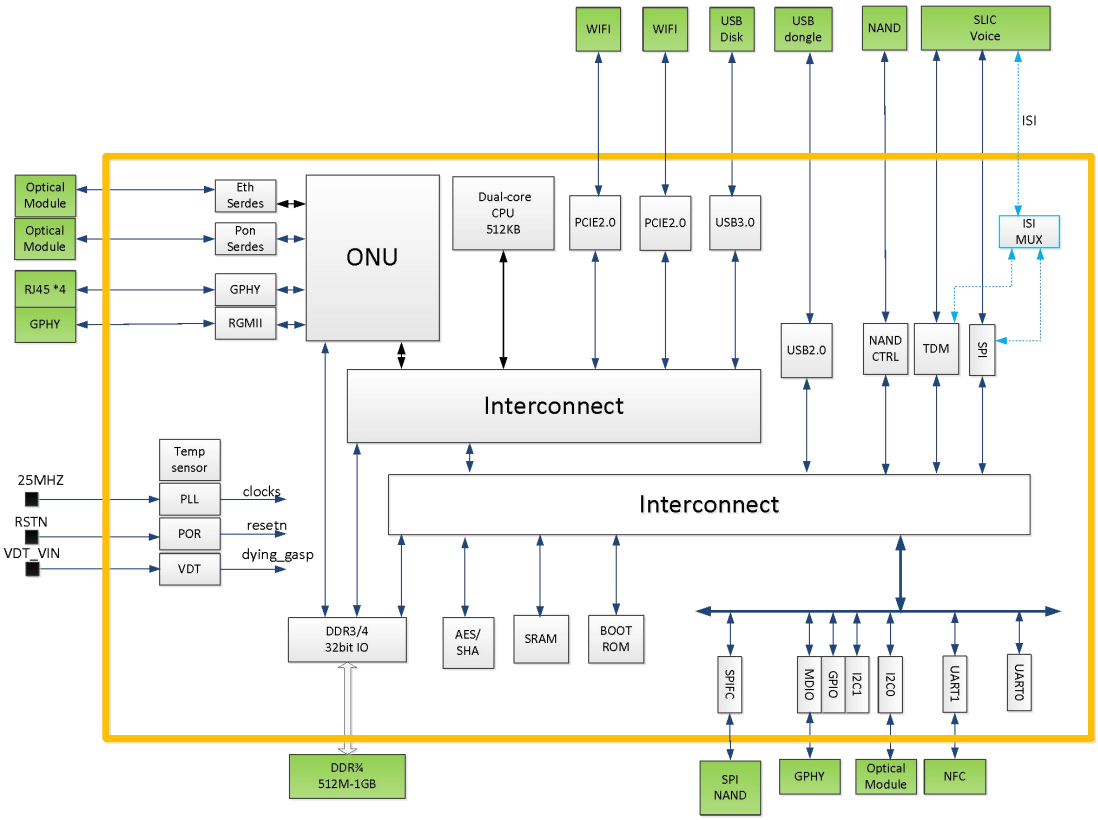


Figure 1-1 Block Diagram

2 Balls

2.1 Ball map

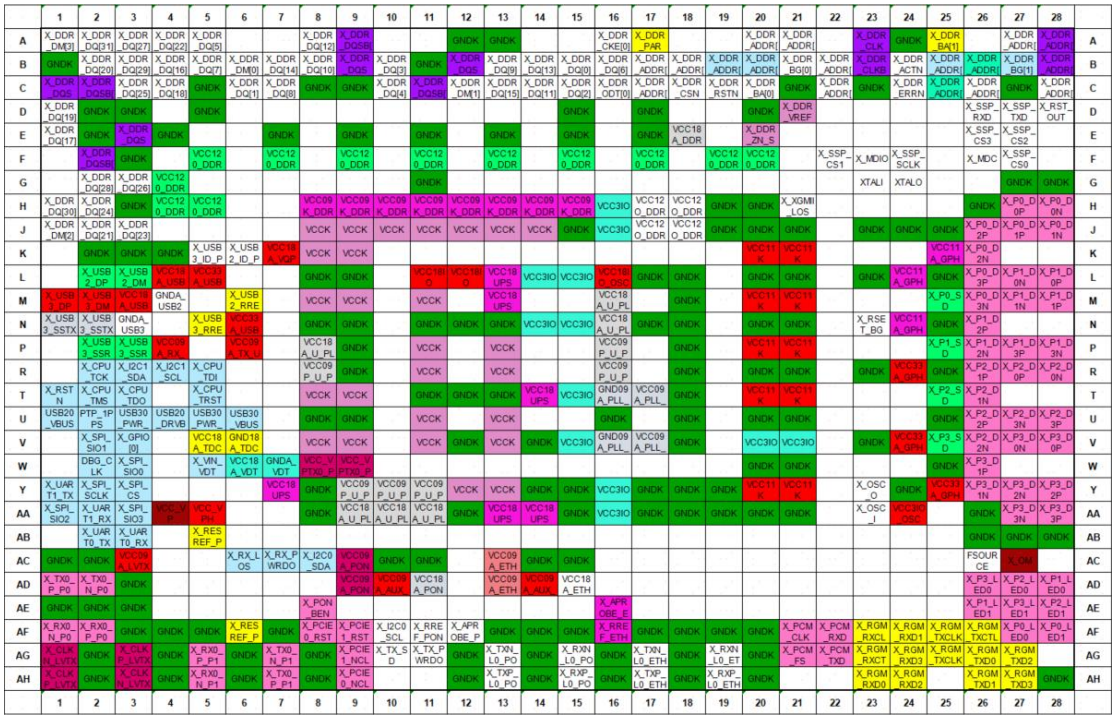


Figure 2-1 5VT2528 Ball Map

2.2 Balls Description

AI ： Analog input

AIO ： Analog input/output

AO ： Analog output

IT ： Input, TTL compatible

OT ： Tristate output, TTL compatible

ITOT ： Input/Output, TTL compatible

SSTL_O：SSTL interface standard output

SSTL_B：SSTL interface standard input/Output

PG ： Power Ground

Table 2-1 MDI Interface Pins

Pin No.	Name	IO Type	Default Value	Description
H28	X_P0_D0N	AIO	Bidirectional Differential IO	MDI[0], Port0. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
H27	X_P0_D0P	AIO	Bidirectional Differential IO	
J28	X_P0_D1N	AIO	Bidirectional Differential IO	MDI[1], Port0. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
J27	X_P0_D1P	AIO	Bidirectional Differential IO	

M25	X_P0_SD	AIO	Bidirectional Differential IO	Fiber mode. Optical detection signal
K6	X_P0_D2N	AIO	Bidirectional Differential IO	MDI[2], Port0. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
J26	X_P0_D2P	AIO	Bidirectional Differential IO	
M26	X_P0_D3N	AIO	Bidirectional Differential IO	MDI[3], Port0. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
L26	X_P0_D3P	AIO	Bidirectional Differential IO	
L27	X_P1_D0N	AIO	Bidirectional Differential IO	MDI[0], Port1. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB ±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
L28	X_P1_D0P	AIO	Bidirectional Differential IO	
M27	X_P1_D1N	AIO	Bidirectional Differential IO	MDI[1], Port1. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA ±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
M28	X_P1_D1P	AIO	Bidirectional Differential IO	
P25	X_P1_SD	AIO	Bidirectional Differential IO	Fiber mode. Optical detection signal
P26	X_P1_D2N	AIO	Bidirectional Differential IO	MDI[2], Port1. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
N26	X_P1_D2P	AIO	Bidirectional Differential IO	
P28	X_P1_D3N	AIO	Bidirectional Differential IO	MDI[3], Port1. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
P27	X_P1_D3P	AIO	Bidirectional Differential IO	
R28	X_P2_D0N	AIO	Bidirectional Differential IO	MDI[0], Port2. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB ±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
R27	X_P2_D0P	AIO	Bidirectional Differential IO	
T26	X_P2_D1N	AIO	Bidirectional Differential IO	MDI[1], Port2. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA ±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
R26	X_P2_D1P	AIO	Bidirectional Differential IO	
T25	X_P2_SD	AIO	Bidirectional Differential IO	Fiber mode. Optical detection signal
V26	X_P2_D2N	AIO	Bidirectional Differential IO	MDI[2], Port2. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
U26	X_P2_D2P	AIO	Bidirectional Differential IO	
U27	X_P2_D3N	AIO	Bidirectional Differential IO	MDI[3], Port2. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC ±; 100Base-TX and 10Base-Te mode can be left

U28	X_P2_D3P	AIO	Bidirectional Differential IO	floating when not in use.
V27	X_P3_D0N	AIO	Bidirectional Differential IO	MDI[0], Port3. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB ±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
V28	X_P3_D0P	AIO	Bidirectional Differential IO	
Y26	X_P3_D1N	AIO	Bidirectional Differential IO	MDI[1], Port3. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA ±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
W26	X_P3_D1P	AIO	Bidirectional Differential IO	
V25	X_P3_SD	AIO	Bidirectional Differential IO	Fiber mode. Optical detection signal
Y27	X_P3_D2N	AIO	Bidirectional Differential IO	MDI[2], Port3. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
Y28	X_P3_D2P	AIO	Bidirectional Differential IO	
AA27	X_P3_D3N	AIO	Bidirectional Differential IO	MDI[3], Port3. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC ±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
AA28	X_P3_D3P	AIO	Bidirectional Differential IO	
N23	X_RSET_BG	AIO	Bidirectional Differential IO	Reference resistor pin, external 3kohm±1% to GND

Table 2-2 DDR Interface Pins

Pin No.	Name	IO Type	Default Value	Description
C22	X_DDR_ADDR[0]	SSTL_O	DDR Analog IO	DDR Address
B26	X_DDR_ADDR[1]	SSTL_O	DDR Analog IO	DDR Address
B28	X_DDR_ADDR[2]	SSTL_O	DDR Analog IO	DDR Address
A28	X_DDR_ADDR[3]	SSTL_O	DDR Analog IO	DDR Address
C25	X_DDR_ADDR[4]	SSTL_O	DDR Analog IO	DDR Address
C28	X_DDR_ADDR[5]	SSTL_O	DDR Analog IO	DDR Address
C26	X_DDR_ADDR[6]	SSTL_O	DDR Analog IO	DDR Address
B19	X_DDR_ADDR[7]	SSTL_O	DDR Analog IO	DDR Address
B22	X_DDR_ADDR[8]	SSTL_O	DDR Analog IO	DDR Address
B20	X_DDR_ADDR[9]	SSTL_O	DDR Analog IO	DDR Address
B17	X_DDR_ADDR[10]	SSTL_O	DDR Analog IO	DDR Address
A27	X_DDR_ADDR[11]	SSTL_O	DDR Analog IO	DDR Address
B25	X_DDR_ADDR[12]	SSTL_O	DDR Analog IO	DDR Address
A20	X_DDR_ADDR[13]	SSTL_O	DDR Analog IO	DDR Address
A21	X_DDR_ADDR[14]	SSTL_O	DDR Analog IO	DDR4: address signal A14; multiplexed as WE_n, low-level active DDR3: WE# only, low-level active

B18	X_DDR_ADDR[15]	SSTL_O	DDR Analog IO	DDR4: address signal A15; multiplexed as CAS_n, low-level active DDR3: CAS# only, low-level active
C17	X_DDR_ADDR[16]	SSTL_O	DDR Analog IO	DDR4: address signal A16; multiplexed as RAS_n, low-level active DDR3: RAS# only, low-level active
B24	X_DDR_ACTN	SSTL_O	DDR Analog IO	DDR3: address signal A15; DDR4: control output ACT_N, active command, low-level active
C20	X_DDR_BA[0]	SSTL_O	DDR Analog IO	DDR3/DDR4: Bank address output[1:0]
A25	X_DDR_BA[1]	SSTL_O	DDR Analog IO	
B21	X_DDR_BG[0]	SSTL_O	DDR Analog IO	DDR3: Bank address output[2] DDR4: Bank Group address output[0]
B27	X_DDR_BG[1]	SSTL_O	DDR Analog IO	DDR3: address signalA14; DDR4: Bank Group address output[1]
A23	X_DDR_CLKB	SSTL_O	DDR Analog IO	DDR3/DDR4 clock output
B23	X_DDR_CLK	SSTL_O	DDR Analog IO	
A16	X_DDR_CKE[0]	SSTL_O	DDR Analog IO	DDR3/DDR4 clock enable output, high-level active
C18	X_DDR_CSN[0]	SSTL_O	DDR Analog IO	DDR3/DDR4 chip select signal output, low-level active
C16	X_DDR_ODT[0]	SSTL_O	DDR Analog IO	DDR3/DDR4 terminal connection resistance enable signal , high-level active
C19	X_DDR_RSTN	SSTL_O	DDR Analog IO	DDR3/DDR4 asynchronous reset output, low-level active
D21	X_DDR_VREF	SSTL_O	DDR Analog IO	
E20	X_DDR_ZN_SENSE	SSTL_O	DDR Analog IO	It is lead out with DDR_ZN and sealed together for DDR3/DDR4 termination reference. It needs to be connected to GND through a 240ohm ±1% resistor.
A17	X_DDR_PAR	SSTL_O	DDR Analog IO	Parity calibration signal
C24	X_DDR_ERRN	SSTL_O	DDR Analog IO	Data reception error signal, low-level active
B6	X_DDR_DM[0]	SSTL_O	DDR Analog IO	Data DQ[7:0]mask; DDR3: high-level active DDR4: low-level active
B12	X_DDR_DQS[0]	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[7:0], DQS, is responsible for the sampling of DQ[7:0]
C11	X_DDR_DQSB[0]	SSTL_O	DDR Analog IO	
B5	X_DDR_DQ[7]	SSTL_B	DDR Analog IO	DDR3/DDR4Data DQ[7:0]
B16	X_DDR_DQ[6]	SSTL_B	DDR Analog IO	
A5	X_DDR_DQ[5]	SSTL_B	DDR Analog IO	
C10	X_DDR_DQ[4]	SSTL_B	DDR Analog IO	
B10	X_DDR_DQ[3]	SSTL_B	DDR Analog IO	
C15	X_DDR_DQ[2]	SSTL_B	DDR Analog IO	
C6	X_DDR_DQ[1]	SSTL_B	DDR Analog IO	
B15	X_DDR_DQ[0]	SSTL_B	DDR Analog IO	
C12	X_DDR_DM[1]	SSTL_O	DDR Analog IO	Data DQ[15:8]mask; DDR3: high-level active DDR4: low-level active

B9	X_DDR_DQS[1]	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[15:8], DQS1, is responsible for the sampling of DQ[15:8]
A9	X_DDR_DQSB[1]	SSTL_O	DDR Analog IO	
C13	X_DDR_DQ[15]	SSTL_B	DDR Analog IO	DDR3/DDR4 Data DQ[15:8]
B7	X_DDR_DQ[14]	SSTL_B	DDR Analog IO	
B14	X_DDR_DQ[13]	SSTL_B	DDR Analog IO	
A8	X_DDR_DQ[12]	SSTL_B	DDR Analog IO	
C14	X_DDR_DQ[11]	SSTL_B	DDR Analog IO	
B8	X_DDR_DQ[10]	SSTL_B	DDR Analog IO	
B13	X_DDR_DQ[9]	SSTL_B	DDR Analog IO	
C7	X_DDR_DQ[8]	SSTL_B	DDR Analog IO	
J1	X_DDR_DM[2]	SSTL_O	DDR Analog IO	Data DQ[23:16]mask; DDR3: high-level active DDR4: low-level active
C1	X_DDR_DQS[2]	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[23:16], DQS1, is responsible for the sampling of DQ[23:16]
C2	X_DDR_DQSB[2]	SSTL_O	DDR Analog IO	
J3	X_DDR_DQ[23]	SSTL_B	DDR Analog IO	DDR3/DDR4 Data DQ[23:16]
A4	X_DDR_DQ[22]	SSTL_B	DDR Analog IO	
J2	X_DDR_DQ[21]	SSTL_B	DDR Analog IO	
B2	X_DDR_DQ[20]	SSTL_B	DDR Analog IO	
D1	X_DDR_DQ[19]	SSTL_B	DDR Analog IO	
C4	X_DDR_DQ[18]	SSTL_B	DDR Analog IO	
E1	X_DDR_DQ[17]	SSTL_B	DDR Analog IO	
B4	X_DDR_DQ[16]	SSTL_B	DDR Analog IO	
A1	X_DDR_DM[3]	SSTL_O	DDR Analog IO	Data DQ[31:24]mask; DDR3: high-level active DDR4: low-level active
E3	X_DDR_DQS[3]	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[31:24], DQS1, is responsible for the sampling of DQ[31:24]
F2	X_DDR_DQSB[3]	SSTL_O	DDR Analog IO	
A2	X_DDR_DQ[31]	SSTL_B	DDR Analog IO	DDR3/DDR4 Data DQ[31:24]
H1	X_DDR_DQ[30]	SSTL_B	DDR Analog IO	
B3	X_DDR_DQ[29]	SSTL_B	DDR Analog IO	
G2	X_DDR_DQ[28]	SSTL_B	DDR Analog IO	
A3	X_DDR_DQ[27]	SSTL_B	DDR Analog IO	
G3	X_DDR_DQ[26]	SSTL_B	DDR Analog IO	
C3	X_DDR_DQ[25]	SSTL_B	DDR Analog IO	
H2	X_DDR_DQ[24]	SSTL_B	DDR Analog IO	

Table 2-3 PON Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AF11	X_RREF_PON	AO	Serdes Analog IO	PON power reference resistor, need to connect 5.6K± 1% to GND
AF12	X_APROBE_PON	AO	Serdes Analog IO	SerDes test pin, can be floated when not in use

AH13	X_TXP_L0_PON	AO	Serdes Differential IO	PON SerDes transmit signal, AC coupling required, 100ohm ±10% differential impedance
AG13	X_TXN_L0_PON	AO	Serdes Differential IO	
AG15	X_RXN_L0_PON	AI	Serdes Differential IO	PON SerDes receive signal, AC coupling required, 100ohm ±10% differential impedance
AH15	X_RXP_L0_PON	AI	Serdes Differential IO	
AF16	X_RREF_ETH	AO	Serdes Analog IO	PON power reference resistor, need to connect 5.6K± 1% to GND
AE16	X_APROBE_ETH	AO	Serdes Analog IO	SerDes test pin, can be floated when not in use
AH17	X_TXP_L0_ETH	AO	Serdes Differential IO	PON SerDes transmit signal, AC coupling required, 100ohm ±10% differential impedance
AG17	X_TXN_L0_ETH	AO	Serdes Differential IO	
AG19	X_RXN_L0_ETH	AI	Serdes Differential IO	PON SerDes receive signal, AC coupling required, 100ohm ±10% differential impedance
AH19	X_RXP_L0_ETH	AI	Serdes Differential IO	
AC7	X_RX_PWRDOWN	ITOT	PULLDOWN	Optical module receive direction power control signal, output high level voltage to turn on the optical module receive direction power, low level voltage to turn off the receive direction power
AG11	X_TX_PWRDOWN	ITOT	PULLUP	Optical module transmit direction power control signal, output high level voltage to turn off the optical module receive direction power, low level voltage to turn on the transmit direction power
AE8	X_PON_BEN	ITOT	NA	Optical module Burst enable signal, polarity can be matched
AC6	X_RX_LOS	ITOT	NA	The optical module receives the detection signal input and connects to the XPON optical module
AG10	X_TX_SD	ITOT	NA	The optical module sends detection signal input
H21	X_XGMII_LOS	ITOT	NA	The optical module receives detection signal input and connects to the ETH optical module

Table 2-4 USB Interface Pins

Pin No.	Name	IO Type	Default Value	Description
K6	X_USB2_ID_PAD	ITOT	USB2.0 Digital IO	USB2.0 ID identification input
L2	X_USB2_DP	AIO	USB2.0 Analog IO	USB2.0 high-speed sending and receiving signals
L3	X_USB2_DM	AIO	USB2.0 Analog IO	
M6	X_USB2_RREF	AIO	USB2.0 Analog IO	USB2 power reference resistor, need to connect 4.7K ±1% to GND
K5	X_USB3_ID_PAD	ITOT	USB3.0 Digital IO	USB3.0 ID identification input
M1	X_USB3_DP	AIO	USB3.0 Analog IO	USB3 high-speed sending and receiving signals
M2	X_USB3_DM	AIO	USB3.0 Analog IO	
N5	X_USB3_RREF	AIO	USB3.0 Analog IO	USB3 power reference resistor, need to connect 4.7K ±1% to GND
N2	X_USB3_SSTXA	AI	USB3.0 Analog IO	USB3 （USB3.x Gen 1） Super high-speed signal reception
N1	X_USB3_SSTXB	AI	USB3.0 Analog IO	

P3	X_USB3_SSRXA	AO	USB3.0 Analog IO	USB3 （USB3.x Gen 1） Super high-speed signal transmission
P2	X_USB3_SSRXB	AO	USB3.0 Analog IO	

Table 2-5 PCIe Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AF2	X_RX0_P_P0	AI	PCIE2.0 Analog IO	PCIe0 SerDes receive signal, AC coupling is required
AF1	X_RX0_N_P0	AI	PCIE2.0 Analog IO	
AD1	X_TX0_P_P0	AO	PCIE2.0 Analog IO	PCIe0 SerDes transmit signal, AC coupling is required
AD2	X_TX0_N_P0	AO	PCIE2.0 Analog IO	
AH1	X_CLKP_LVTX	AO	PCIE2.0 Analog IO	PCIe0 100MHz reference clock output
AG1	X_CLKN_LVTX	AO	PCIE2.0 Analog IO	
AH9	X_PCIE0_NCLKREQ	ITOT	NA	PCIe0 CLKREQ signal
AB5	X_RESREF_P0	AIO	PCIE2.0 Analog IO	PCIe0 reference resistor, need to connect 200ohm ±1% to GND
AF8	X_PCIE0_RSTN	ITOT	NA	PCIe0 reset output
AG5	X_RX0_P_P1	AI	PCIE2.0 Analog IO	PCIe1 SerDes receive signal, AC coupling is required
AH5	X_RX0_N_P1	AI	PCIE2.0 Analog IO	
AH7	X_TX0_P_P1	AO	PCIE2.0 Analog IO	PCIe1 SerDes transmit signal, AC coupling is required
AG7	X_TX0_N_P1	AO	PCIE2.0 Analog IO	
AG3	X_CLKP_LVTX_1	AO	PCIE2.0 Analog IO	PCIe1 100MHz reference clock output
AH3	X_CLKN_LVTX_1	AO	PCIE2.0 Analog IO	
AG9	X_PCIE1_NCLKREQ	ITOT	NA	PCIe1 CLKREQ signal
AF6	X_RESREF_P1	AIO	PCIE20 Analog IO	PCIe1 reference resistor, need to connect 200ohm ± 1% to GND
AF9	X_PCIE1_RSTN	ITOT	NA	PCIe1 reset output

Table 2-6 SPIFC Interface Pins

Pin No.	Name	IO Type	Default Value	Description
W3	X_SPI_SIO0	ITOT	NA	SPI Flash D0
V2	X_SPI_SIO1	ITOT	NA	SPI Flash D1
AA1	X_SPI_SIO2	ITOT	NA	SPI Flash D2
AA3	X_SPI_SIO3	ITOT	NA	SPI Flash D3
Y2	X_SPI_SCLK	ITOT	NA	SPI Flash clock output
Y3	X_SPI_CS	ITOT	NA	SPI Flash chip select

Table 2-7 JTAG Interface Pins

Pin No.	Name	IO Type	Default Value	Description
T5	X_CPU_TRSTN	ITOT	PULLDOWN	Debug interface reset
T3	X_CPU_TDO	ITOT	NA	Debug interface data output
R2	X_CPU_TCK	ITOT	PULLDOWN	Debug interface clock
R5	X_CPU_TDI	ITOT	PULLUP	Debug interface data input

T2	X_CPU_TMS	ITOT	PULLUP	Debug interface mode selection

Table 2-8 SPI Interface Pins

Pin No.	Name	IO Type	Default Value	Description
F27	X_SSP_CS0	ITOT	NA	SPI select signal, can be used as SPI interface in PCM mode
F22	X_SSP_CS1	ITOT	NA	
E27	X_SSP_CS2	ITOT	NA	
E26	X_SSP_CS3	ITOT	NA	
D26	X_SSP_RXD	ITOT	NA	SPI receives data, can be used as SPI interface in PCM mode
F24	X_SSP_SCLK	ITOT	NA	SPI clock output, can be used as SPI interface in PCM mode
D27	X_SSP_TXD	ITOT	NA	SPI transmit data, can be used as SPI interface in PCM mode

Table 2-9 PCM Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AF21	X_PCM_CLK	ITOT	NA	PCM clock output
AG21	X_PCM_FS	ITOT	NA	PCM sync frame signal, ISI mode can be left floating
AF22	X_PCM_RXD	ITOT	NA	PCM receive signal
AG22	X_PCM_TXD	ITOT	NA	PCM transmit signal

Table 2-10 RGMII Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AF23	X_RGM_RXCLK	ITOT	NA	RGMII interface receive clock
AG23	X_RGM_RXCTL	ITOT	NA	RGMII interface receive control
AH23	X_RGM_RXD0	ITOT	NA	RGMII interface receive data
AF24	X_RGM_RXD1	ITOT	NA	RGMII interface receive data
AH24	X_RGM_RXD2	ITOT	NA	RGMII interface receive data
AG24	X_RGM_RXD3	ITOT	NA	RGMII interface receive data
AF25	X_RGM_TXCLK	ITOT	NA	RGMII interface transmit clock
AG25	X_RGM_TXCLK_IN	ITOT	NA	MII mode clock input, can be floated when not in use
AF26	X_RGM_TXCTL	ITOT	NA	RGMII interface transmit control
AG26	X_RGM_TXD0	ITOT	NA	RGMII interface transmit data
AH26	X_RGM_TXD1	ITOT	NA	RGMII interface transmit data
AG27	X_RGM_TXD2	ITOT	NA	RGMII interface transmit data
AH27	X_RGM_TXD3	ITOT	NA	RGMII interface transmit data

Table 2-11 Other Interface Pins

Pin No.	Name	IO Type	Default Value	Description
G23	XTALI	AI	-	Crystal IO input terminal, external 25MHZ crystal oscillator circuit
G24	XTALO	AO	-	Crystal IO output terminal, external 25MHZ crystal oscillator circuit
Y23	X_OSC_I	AI		Reserve
AA23	X_OSC_O	AO		Reserve
W5	X_VIN_VDT	AI		Dying Gasp analog input
AC27	X_OM	IT	PULLDOWN	Test mode configuration, 0: chip works normally, 1: chip test mode
AB3	X_UART0_RX	ITOT	PULLUP	UART0 receive signal pin
AB2	X_UART0_TX	ITOT	NA	UART0 send signal pin
AA2	X_UART1_RX	ITOT	PULLUP	UART1 receive signal pin
Y1	X_UART1_TX	ITOT	NA	UART1 send signal pin
AF10	X_I2C0_SCL	ITOT	PULLUP	I2C0 clock output signal, need external pull-up resistor
AC8	X_I2C0_SDA	ITOT	PULLUP	I2C0 data transmission and reception signal, need external pull-up resistor
R4	X_I2C1_SCL	ITOT	PULLUP	I2C1clock output signal, need external pull-up resistor
R3	X_I2C1_SDA	ITOT	PULLUP	I2C1data transmission and reception signal, need external pull-up resistor
AF27	X_P0_LED0	ITOT	NA	GEPHY Port0 LED0, function register configurable
AF28	X_P0_LED1	ITOT	NA	GEPHY Port0 LED1, function register configurable
AD28	X_P1_LED0	ITOT	NA	GEPHY Port1 LED0, function register configurable
AE26	X_P1_LED1	ITOT	NA	GEPHY Port1 LED1, function register configurable
AD27	X_P2_LED0	ITOT	NA	GEPHY Port2 LED0, function register configurable
AE28	X_P2_LED1	ITOT	NA	GEPHY Port2 LED1, function register configurable
AD26	X_P3_LED0	ITOT	NA	GEPHY Port3 LED0, function register configurable
AE27	X_P3_LED1	ITOT	NA	GEPHY Port3 LED1, function register configurable
T1	X_RSTN	ITOT	PULLUP	Chip hardware reset input, requires an external reset circuit or pull-up resistor.
D28	X_RST_OUT	ITOT	NA	Chip reset output
V3	X_GPIO[0]/EXT_RST_N	ITOT	NA	Normal GPIO
U3	X_GPIO[1]/USB30_PWR_OC	ITOT	NA	Normal GPIO(USB3.0 power overcurrent detection input)
U2	X_GPIO[2]/PTP_1PPS	ITOT	NA	Normal GPIO(PTP timestamp signal output)
U1	X_GPIO[3]/USB20_VBUS_CTRL	ITOT	NA	Normal GPIO(USB2.0 VBUS detection input)
U4	X_GPIO[4]/USB20_DRVBUS	ITOT	NA	Normal GPIO(USB2.0 VBUS power supply control enable)
U6	X_GPIO[5]/USB30	ITOT	NA	Normal GPIO(USB3.0 VBUS detection input)

	_VBUS			
U5	X_GPIO[6]/USB30_PWR_EN	ITOT	NA	Normal GPIO(USB3.0 VBUS power supply control enable)
W2	X_GPIO[7]/DBG_CLK	ITOT	NA	Normal GPIO(DEBUG CLOCK OUTPUT)
F26	X_MDC	ITOT	NA	Management Data Clock
F23	X_MDIO	ITOT	PULLUP	Management Data Input/Output (MDIO)
K7	VQPS_EFUSE	AIO	NA	Test pin, floating
AC26	FSOURCE	AIO	NA	Test pin, floating

Table 2-12 Power Ground

Pin No.	Quantity	Name	IO Type	Description
H16,J16,L14,L15,N14,N15,T15,V15,V20,V21,Y16,AA16	12	VCC3IO	PG	3.3V IO digital power
AA24	1	VCC3IO_OSC	PG	3.3V OSC digital power
R24,V24,Y25	3	VCC33A_GPHY	PG	GPHY 3.3V analog power
F5 ,F7 ,F9 ,F11,F13,F15,F17,F19,F20,G4 ,H4,H5	12	VCC120_DDR	PG	DDR3/DDR4 PHY IO power: DDR3: connect to 1.5V DDR4: connect to 1.2V
H17,H18,J17,J18	4	VCC12O_DDRCK	PG	DDR3/DDR4 PHY CK IO power: DDR3: connect to 1.5V DDR4: connect to 1.2V
E18	1	VCC18A_DDR_PLL	PG	1.8V DDRPHY PLL analog power
H8,H9,H10,H11,H12,H13,H14,H15	8	VCC09K_DDR_PHY	PG	DDRPHY 0.9V digital power
K20,K21,M20,M21,P20,P21,T20,T21,Y20,Y21	10	VCC11K	PG	GPHY 1.1V core digital power
K25,L24,N24	3	VCC11A_GPHY	PG	GPHY 1.1V analog power
J8 ,J9 ,J10,J11,J12,J13,J14,K8 ,K9 ,M8 ,M9 ,M11,P11,P13,R11,R13,T8 ,T9 ,U11,U13,V8 ,V9 ,V11,V13,Y12,Y13	26	VCCK	PG	0.9V core digital power
L13,M13,T14,Y7,AA13,AA14	6	VCC18UPS	PG	Multi-Voltage IO 1.8V Digital Power
L11,L12	2	VCC18IO	PG	1.8V IO digital power
L16	1	VCC18IO_OSC	PG	1.8V OSC digital power
AC9,AD9	2	VCC09A_PON	PG	0.9V PON analog power
AC13,AD13	2	VCC09A_ETH	PG	0.9V ETH analog power
AA4	1	VCC_VP	PG	0.9V PCIePHY analog power

AA5	1	VCC_VPH	PG	1.8V PCIePHY analog power
W9	1	VCC_VPTX0_P0	PG	0.9V PCIePHY analog transmit power
W8	1	VCC_VPTX0_P1	PG	0.9V PCIePHY analog transmit power
AD14	1	VCC09A_AUX_ETH	PG	0.9V serdes auxiliary analog power
AD10	1	VCC09A_AUX_PON	PG	0.9V serdes auxiliary analog power
AC3	1	VCC09A_LVTX	PG	0.9V differential IO analog power
V17	1	VCC09A_PLL_BUS	PG	0.9V PLL Analog power
T17	1	VCC09A_PLL_CPU	PG	0.9V PLL Analog power
P4	1	VCC09A_RX_USB3	PG	0.9V PLL Analog power
P6	1	VCC09A_TX_USB3	PG	0.9V PLL Analog power
R16	1	VCC09P_U_PLL_DDR	PG	0.9V PLL Analog power
Y11	1	VCC09P_U_PLL_ETH	PG	0.9V PLL Analog power
Y9	1	VCC09P_U_PLL_PON	PG	0.9V PLL Analog power
Y10	1	VCC09P_U_PLL_SYNC	PG	0.9V PLL Analog power
P16	1	VCC09P_U_PLL_TDM	PG	0.9V PLL Analog power
R8	1	VCC09P_U_PLL_USB	PG	0.9V PLL Analog power
AD15	1	VCC18A_ETH	PG	1.8V serdes Analog power
AD11	1	VCC18A_PON	PG	1.8V serdes Analog power
V5	1	VCC18A_TDC	PG	1.8V TDC Analog power
M16	1	VCC18A_U_PLL_DDR	PG	1.8V PLL Analog power
AA11	1	VCC18A_U_PLL_ETH	PG	1.8V PLL Analog power
AA9	1	VCC18A_U_PLL_PON	PG	1.8V PLL Analog power
AA10	1	VCC18A_U_PLL_SYNC	PG	1.8V PLL Analog power
N16	1	VCC18A_U_PLL_TDM	PG	1.8V PLL Analog power
P8	1	VCC18A_U_PLL_USB	PG	1.8V PLL Analog power
L4	1	VCC18A_USB2	PG	1.8V USB 2.0PHY Analog

				power
M3	1	VCC18A_USB3	PG	1.8V USB 3.0PHY Analog power
W6	1	VCC18A_VDT	PG	1.8V VDT Analog power
L5	1	VCC33A_USB2	PG	3.3V USB2.0 PHY Analog power
N6	1	VCC33A_USB3	PG	3.3V USB3.0 PHY Analog power
A12 ,A13 ,A24 ,B1 ,B11 ,C5 ,C8 ,C9 ,C21 ,C23 ,C27 ,D2 ,D3 ,D5 ,D15 , D17 ,D20 ,E2 ,E4 ,E7 ,E9 ,E11 ,E13 ,E15 ,E17 ,F3 ,G11 ,G27 ,G28 ,H3 , H19 ,H20 ,H26 ,J15 ,J19 ,J20 ,J21 ,J23 ,J24 ,J25 ,K2 ,K3 ,K4 ,L8 ,L9 , L17 ,L18 ,L20 ,L21 ,L23 ,L25 ,M18 ,N8 ,N9 , N11 ,N12 ,N13 ,N17 ,N18 ,N20 , N21 ,N25 ,P9 ,P18 ,R9 ,R18 ,R20 ,R21 ,R23 ,R25 ,T11 ,T12 ,T13 ,T18 ,U8 , U9 ,U16 ,U18 ,U20 ,U21 ,U25 ,V12 ,V14 ,V18 ,V23 ,W20 ,W21 ,W25 ,Y8 ,Y14 , Y15 ,Y17 ,Y18 ,Y19 ,Y24 ,AA8 ,AA12,AA15,AA17,AA18,AA19,AA20,AA21,AA26,AB26, AB27,AB28,AC1 ,AC2 ,AC10,AC11,AC14,AC15, AD3 ,AE1 ,AE2 ,AE3 ,AF3 ,AF4 ,AF5 , AF7 ,AF13,AF14,AF15,AF17,AF18,AF19,AF20, AG2 ,AG4 ,AG6 ,AG8 ,AG12,AG14,AG16, AG18,AG20,AH2 ,AH4 ,AH6 ,AH8 ,AH12,AH14, AH16,AH18,AH20,AH28	147	GNDK	PG	Power/Ground
V16	1	GND09A_PLL_BUS	PG	Power/Ground
T16	1	GND09A_PLL_CPU	PG	Power/Ground
V6	1	GND18A_TDC	PG	Power/Ground
M4	1	GNDA_USB2	PG	Power/Ground
N3	1	GNDA_USB3	PG	Power/Ground
W7	1	GNDA_VDT	PG	Power/Ground

Notes

The pull-up and pull-down resistor values:

PULLUP: 40-kΩ

PULLDOWN: 40-kΩ

NA: By default, there is no pull-up and drop-down settings

2.3 Pin Sharing Schemes

Table 2-13 GPIO Multiplexed Pin Options

Pin No.	Name	Default Function		2nd Function		3rd Function	
		Name	Direction	Name	Direction	Name	Direction
T5	X_CPU_TRSTn	X_CPU_TRSTn	IN	UART2_RTS	OUT	GPIO_0	INOUT
R2	X_CPU_TCK	X_CPU_TCK	IN	UART2_RXD	IN	GPIO_1	INOUT
T2	X_CPU_TMS	X_CPU_TMS	IN	UART2_CTS	IN	GPIO_2	INOUT
R5	X_CPU_TDI	X_CPU_TDI	IN	DYING_GASPOUT	OUT	GPIO_3	INOUT
T3	X_CPU_TDO	X_CPU_TDO	OUT	UART2_TXD	OUT	GPIO_4	INOUT
AG25	X_RGM_TXCLK_IN	X_RGM_TXCLK_IN	IN	DYING_GASPIN	IN	GPIO_5	INOUT
AG10	X_TX_SD	X_TX_SD	IN			GPIO_6	INOUT
AC6	X_RX_LOS	X_RX_LOS	IN			GPIO_7	INOUT
AE8	X_PON_BEN	X_PON_BEN	OUT			GPIO_8	INOUT
AG11	X_TX_PWRDOWN	X_TX_PWRDOWN	OUT			GPIO_9	INOUT
AC7	X_RX_PWRDOWN	X_RX_PWRDOWN	OUT			GPIO_10	INOUT
H21	X_XGMII_LOS	X_XGMII_LOS	OUT	CLK8K_OUT	OUT	GPIO_11	INOUT
Y2	X_SPI_SCLK	X_SPI_SCLK	OUT	NAND_CEN	OUT	GPIO_12	INOUT
Y3	X_SPI_CS	X_SPI_CS	OUT	NAND_REN	OUT	GPIO_13	INOUT
W3	X_SPI_SIO0	X_SPI_SIO0	INOUT	NAND_CLE	OUT	GPIO_14	INOUT
V2	X_SPI_SIO1	X_SPI_SIO1	INOUT	NAND_WEN	OUT	GPIO_15	INOUT
AA1	X_SPI_SIO2	X_SPI_SIO2	INOUT	NAND_ALE	OUT	GPIO_16	INOUT
AA3	X_SPI_SIO3	X_SPI_SIO3	INOUT	NAND_BUSY_N	IN	GPIO_17	INOUT
AF25	X_RGM_TXCLK	X_RGM_TXCLK	OUT	NAND_DATA0	INOUT	GPIO_18	INOUT
AF26	X_RGM_TXCTL	X_RGM_TXCTL	OUT	NAND_DATA1	INOUT	GPIO_19	INOUT
AG26	X_RGM_TXD0	X_RGM_TXD0	OUT	NAND_DATA2	INOUT	GPIO_20	INOUT
AH26	X_RGM_TXD1	X_RGM_TXD1	OUT	NAND_DATA3	INOUT	GPIO_21	INOUT
AG27	X_RGM_TXD2	X_RGM_TXD2	OUT	NAND_DATA4	INOUT	GPIO_22	INOUT
AH27	X_RGM_TXD3	X_RGM_TXD3	OUT	NAND_DATA5	INOUT	GPIO_23	INOUT
AH23	X_RGM_RXD0	X_RGM_RXD0	IN	NAND_DATA6	INOUT	GPIO_24	INOUT
AF24	X_RGM_RXD1	X_RGM_RXD1	IN	NAND_DATA7	INOUT	GPIO_25	INOUT
AH24	X_RGM_RXD2	X_RGM_RXD2	IN			GPIO_26	INOUT
AG24	X_RGM_RXD3	X_RGM_RXD3	IN			GPIO_27	INOUT
AG23	X_RGM_RXCTL	X_RGM_RXCTL	IN			GPIO_28	INOUT
AF23	X_RGM_RXCLK	X_RGM_RXCLK	IN			GPIO_29	INOUT
AF21	X_PCM_CLK	X_PCM_CLK	OUT	ISI_PSCLK	OUT	GPIO_30	INOUT
AG21	X_PCM_FS	X_PCM_FS	OUT			GPIO_31	INOUT
AG22	X_PCM_TXD	X_PCM_TXD	OUT	ISI_MOSI	OUT	GPIO_0	INOUT
AF22	X_PCM_RXD	X_PCM_RXD	IN	ISI_MISO	IN	GPIO_1	INOUT
AB3	X_UART0_RX	X_UART0_RX	IN			GPIO_2	INOUT
AB2	X_UART0_TX	X_UART0_TX	OUT			GPIO_3	INOUT
AA2	X_UART1_RX	X_UART1_RX	IN	PON_BEN_INV	OUT	GPIO_4	INOUT

Y1	X_UART1_TX	X_UART1_TX	OUT			GPIO_5	INOUT
AF10	X_I2C0_SCL	X_I2C0_SCL	INOUT			GPIO_6	INOUT
AC8	X_I2C0_SDA	X_I2C0_SDA	INOUT			GPIO_7	INOUT
R4	X_I2C1_SCL	X_I2C1_SCL	INOUT	GMII_TXER	OUT	GPIO_8	INOUT
R3	X_I2C1_SDA	X_I2C1_SDA	INOUT	GMII_RXER	IN	GPIO_9	INOUT
F27	X_SSP_CS0	X_SSP_CS0	OUT			GPIO_10	INOUT
F22	X_SSP_CS1	X_SSP_CS1	OUT			GPIO_11	INOUT
E27	X_SSP_CS2	X_SSP_CS2	OUT			GPIO_12	INOUT
E26	X_SSP_CS3	X_SSP_CS3	OUT			GPIO_13	INOUT
D27	X_SSP_TXD	X_SSP_TXD	OUT			GPIO_14	INOUT
D26	X_SSP_RXD	X_SSP_RXD	IN			GPIO_15	INOUT
F24	X_SSP_SCLK	X_SSP_SCLK	OUT			GPIO_16	INOUT
F26	X_MDC	X_MDC	OUT			GPIO_17	INOUT
F23	X_MDIO	X_MDIO	INOUT			GPIO_18	INOUT
D28	X_RST_OUT	X_RST_OUT	OUT			GPIO_19	INOUT
AF8	X_PCIe0_RST	X_PCIe0_RST	OUT			GPIO_20	INOUT
AH9	X_PCIe0_nCLKREQ	X_PCIe0_nCLKREQ	IN			GPIO_21	INOUT
AF9	X_PCIe1_RST	X_PCIe1_RST	OUT			GPIO_22	INOUT
AG9	X_PCIe1_nCLKREQ	X_PCIe1_nCLKREQ	IN			GPIO_23	INOUT
V3	EXT_RST_N	EXT_RST_N	OUT			GPIO_24	INOUT
U3	USB30_PWR_OC	USB30_PWR_OC	IN			GPIO_25	INOUT
U2	PTP_1PPS	PTP_1PPS	OUT			GPIO_26	INOUT
U1	USB20_VBUS_CTRL	USB20_VBUS_CTRL	IN			GPIO_27	INOUT
U4	USB20_DRVBUS	USB20_DRVBUS	OUT			GPIO_28	INOUT
U6	USB30_VBUS	USB30_VBUS	IN			GPIO_29	INOUT
U5	USB30_PWR_EN	USB30_PWR_EN	OUT			GPIO_30	INOUT
W2	DBG_CLK	DBG_CLK	OUT			GPIO_31	INOUT

Notes: The GPIO module actually has only 32 GPIOs, which are multiplexed into two groups of 32 pins. The actual number of GPIOs available at the same time is 32 instead of 64.

3 BOOT Mode

Support four Boot mode as followed:

Table 3-1 Boot mode

Name	Selection			
STRAP_BOOT_MODE0 (X_SSP_TXD)	0	0	1	1
STRAP_BOOT_MODE1	0	1	0	1

(X_SSP_CS0)				
Boot Mode	UART0 boot	SPI NOR boot	SPI NAND boot	Parallel NAND boot

Table 3-2 Boot parameter

STRAP_NAND_PAGE_SIZE (X_SSP_CS1)	0:2K bytes 1:4K bytes
STRAP_NAND_ADDR_CYC (X_SSP_CS2)	Parallel NAND/SPI NAND 0:2-cycle/3-byte mode 1:3-cycle/4-byte mode
STRAP_XIP_SEL (X_SSP_RXD)	0:BOOT From BOOTROM 1:BOOT From SPI XIP
STRAP_NAND_ECC (X_SSP_CS3)	NAND 0:ECC 4-bit 1:ECC 8-bit

4 Features Description

4.1 SOC Subsystem

4.1.1 Processor

The chip has a built-in dual-core 64-bit high-performance processor with 32KB L1 cache, 512KB L2 cache and a maximum operating frequency of 1Ghz, which can meet various business applications.

4.1.2 DDR3/4

The system integrates a DDR3/DDR4 combo controller and PHY, supporting the following features:

☐ Supports 32-bit IO width

☐ Supports DDR3-1600Mbps

☐ Supports DDR4-2133Mbps

4.1.3 PCIE2.0

The chip supports 2 PCIE2.0 interfaces with a maximum rate of 5Gbps and can be plugged into a WIFI chip for WIFI5/6 access.

4.1.4 USB3.0

The chip integrates a USB3.0 controller and supports the following features:

☐ USB3.0 host mode

☐ Supports USB3.0 device, device mode is option

☐ Supports USB2.0 and USB1.1 devices through hub extension

☐ Supports low power consumption mode

4.1.5 USB2.0

The chip integrates a USB2.0 controller and supports the following features:

☐ USB2.0 host mode

☐ Support USB2.0 device, device mode is option

☐ Compatible with USB1.1 devices

☐ Supports low power consumption mode

4.1.6 NAND

The chip supports parallel port NAND devices:

☐ Supports standard compatible ONFI NAND devices, including ONFI3 and below

☐ Supports maximum capacity 4GB

☐ block size supports 8K~2048KB

☐ Page sizes support 512B~8KB, but do not support 512B when booting

☐ Maximum support ECC error correction to 8bit

4.1.7 SPIFC

The chip integrates SPI flash controller to realize external Norflash or Nandflash device.

☐ Supports DTR mode

☐ Supports DUAL/QUAD output mode, also supports DUAL/QUAD IO mode

☐ Support SPI working frequency programmable setting

☐ Support SPI NOR/NAND command port command mode

4.1.8 GPIO

Programmable general purpose IO controllers that can be programmed for each GPIO pin to meet differentiated requirements.

☐ Support for up to 32 GPIOs programmable

☐ 32 GPIOs can all trigger GPIO interrupts independently

☐ Interrupts of the GPIOs that support interrupts all support edge-triggered, level-triggered
☐ Each GPIO can supports configuration to high or low level
☐ Each GPIO output data is independently set or cleared
☐ All GPIO ports can be set as inputs after a hardware reset

4.1.9 I2C

The I2C module supports CPU configuration in master mode or slave mode.
☐ Supports I2C standard mode, fast mode and fast + mode
☐ Supports HS high-speed mode
☐ Supports 7/10bit address searching
☐ Supports Glitch-Free
☐ Supports programmable slave address
☐ Support master-TX, master-RX, slave-TX and slave-RX modes

4.1.10 UART

UART is an asynchronous serial communication control module and supports infrared control mode.. It is compatible with 16550 protocol.
☐ Compatible with high-speed NS 16550A protocol
☐ Supports infrared 1.3 SIR, the rate can reach 115kbps
☐ Supports programmable SIR pulse width of 1.6us or 3/16 baud rate pulse width
☐ Supports multi-frame transmission mechanism in FIR mode
☐ Supports interrupt, polarity, overflow and frame error emulation

4.1.11 WDT

In the conventional WDT design, in order to prevent the CPU software from entering a deadlock, when the software cannot input WatchDog Timer regularly, the system can be reset so that it can be restarted.

☐ After timing out, the following signals can be output
  1）System reset
  2）System interruption
  3）External interrupt
☐ 32-bit down counter
☐ Internal or external clock source can be selected
☐ Output reset width period is configurable

☐ Access protection registers are set

4.1.12 TIMER

The timer module provides 4 sub-timer settings, which are independent of each other. Whether to issue a timer interrupt depends on the register settings.
☐ four sub-settings for 32-bit timing configurations
☐ The timing clock is 25Mhz
☐ Issue an interrupt after overflow and the timer is reached
☐ Support timed increment or decrement

4.1.13 MDIO

Used to control the external GEPHY two-wire interface.

4.1.14 TDM/SPI/ISI

Voice interface, two working modes:
TDM+SPI mode: use 4 lines of TDM and SPI to connect with SLIC chip to realize voice communication
ISI mode: use ISI interface 3 lines to connect with SLIC chip to realize voice communication.

4.2 ONU Subsystem

The chip supports GPON/EPON/XGPON/XEPON/XGSPON multi-mode fibre access, while implementing SOC chips for Layer 2 switching and Layer 3/4 hardware NAT/NAPT functions; Equipped with 4-channel Ethernet port + 1-channel RGMII/SGMII/HSGMII + 1-channel XFI, supports DDR3/DDR4 particles, supports WIFI access through PCIE interface with external WIFI chip, realizes the function of low-cost home optical modem and gateway in one. The chip supports L2 and supports L3 NAT/NAPT hardwired network switching. The chip can be used for a variety of service applications on the upper layer of the processor, such as DHCP, HTTP and some services that require the use of hardwired forwarding functions.

The chip has an integrated GPON/EPON/XGPON/XEPON/XGSPON engine to support network bridging and routing services for handling ultra-low cost optical network terminals.

The chip has built-in powerful protocol analysis functions and can handle various hard forwarding

services such as VLAN, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP messages. For VLAN and PPPoE protocols, the chip supports automatic encapsulation and decapsulation of VLAN tagged frames and PPPoE headers.

The chip supports port-based, protocol-based, VLAN-based, etc. It supports up to 4,000 VLAN groups and supports the SPAN tree protocol, whose states can be divided into four: forbidden, blocking, listening and forwarding.

5 Interface Timing and Characteristics

5.1 SPI Interface Timing

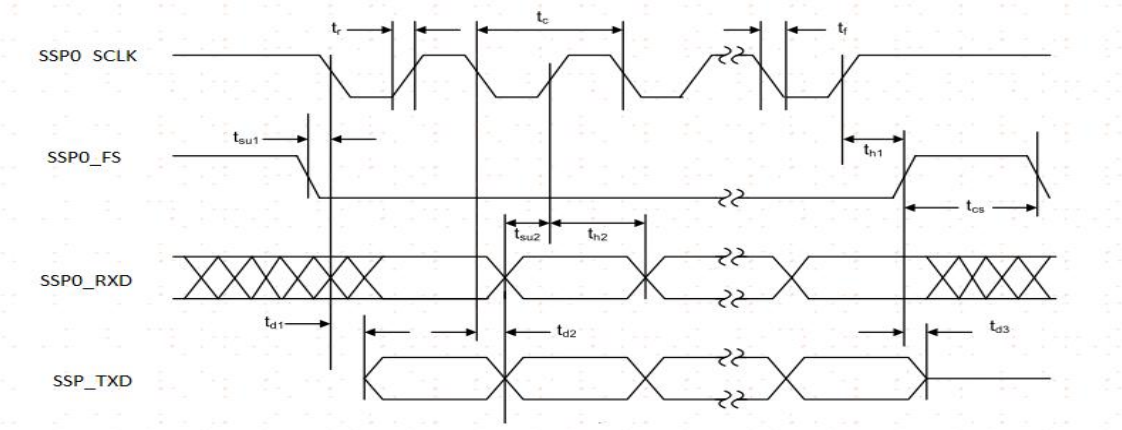


Figure 5-1 SPI Interface Timing

Table 5-1

Symbol	Parameter	Min.	Typ.	Max.	Units
Tc	Cycle time SSP0_SCLK	62	--	--	ns
Tr	Rise time of SSP0_SCLK	--	--	25	ns
Tf	Fall time of SSP0_SCLK	--	--	25	ns
Td1	Delay time,SSP0_SCLK fall to SSP0_TXD active	--	--	20	ns
Td2	Delay time,SSP0_SCLK fall to SSP0_TXD transition	--	--	20	ns
Td3	Delay time,SSP0_FS rise to SSP0_TXD tristate	--	--	20	ns
Tsu1	Setup time,SSP0_FS to SSP0_SCLK fall	25	--	--	ns
Th1	Hold time,SSP0_FS to SSP0_SCLK rise	20	--	--	ns
Tsu2	Setup time,SSP0_RXD to SSP0_SCLK rise	25	--	--	ns
Th2	Hold time,SSP0_RXD to SSP0_SCLK rise	20	--	--	ns
Tcs	Delay time between chip selects	220	--	--	ns

5.2 JTAG Interface Timing

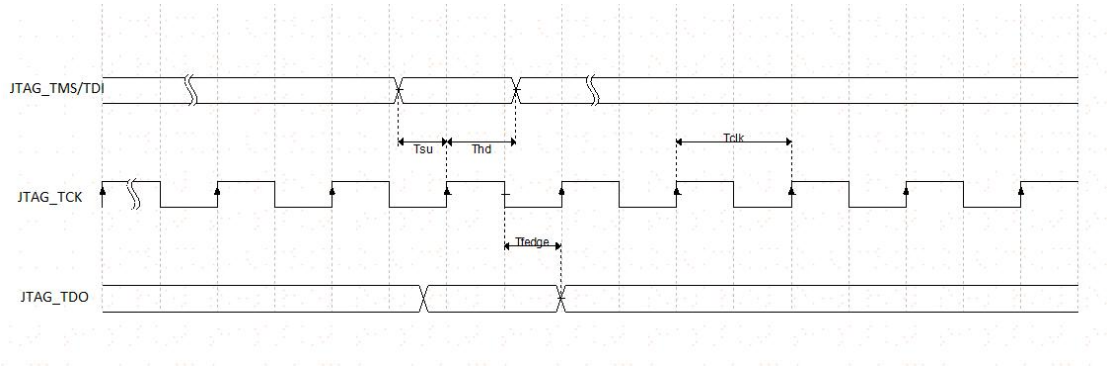


Figure 5-2 JTAG Interface Timing

Table 5-2

Symbol	Parameter	Min.	Typ.	Max.	Units
Tclk	JTAG_TCK clock cycle	100	200	-	ns
Tsu	Setup time for input	10	-	-	ns
Thd	Hold time for input	10	-	-	ns
Tdly	Delay time for output	-		20	ns

5.3 MDIO Interface Timing

Receive:

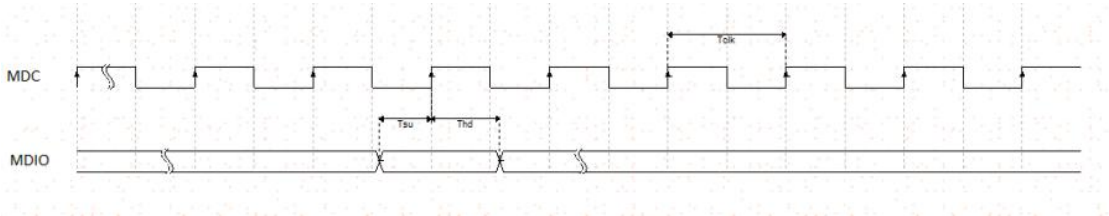


Figure 5-3 MDIO Interface Receive Timing

Transmit:

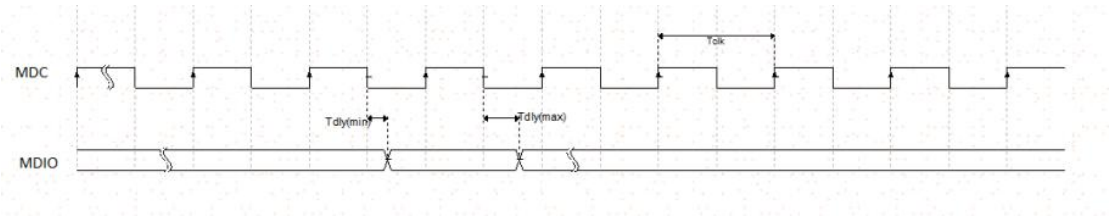


Figure 5-4 MDIO Interface Transmit Timing

Table 5-3

Symbol	Parameter	Min.	Typ.	Max.	Units
Tclk	MDC clock cycle	2500	2000	-	ns
Tsu	Setup time for input	10	-	-	ns
Thd	Hold time for input	10	-	-	ns
Tdly	Delay time for output	--		1000	ns

5.4 I2C Interface Timing

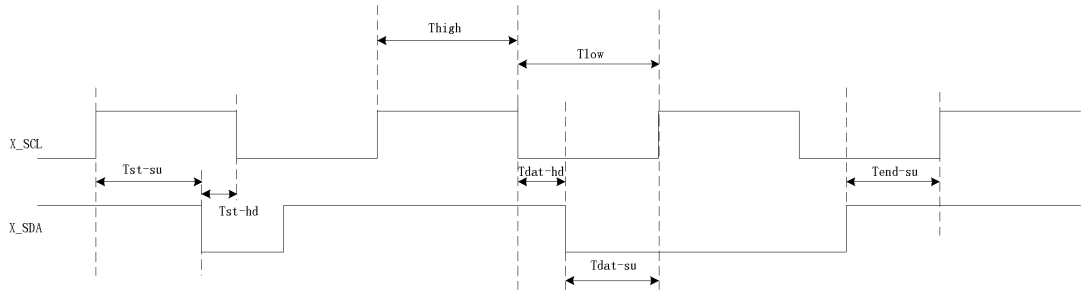


Figure 5-5 I2C Interface Timing

Table 5-4

Symbol	Parameter	Standard mode		Fast mode		Units
		Min.	Max.	Min.	Max.	
fscl	Clock frequency		100		400	Khz
Tlow	Clock low-level voltage time	4.7		1.3		us
Thigh	Clock high-level voltage time	4.0		0.6		us
Tst-su	Setup time for start	4.7		0.6		us
Tst-hd	hold time for start	4.0		0.6		us
Tdat-su	Setup time for data	250		100		ns
Tdat-hd	Hold time for data	5.0	3.45	0	0.9	us
Tend-su	Setup time for end	4.0		0.6		us

Note：Tdat-hd uses the Max value(3.45us) only when the SCL Tlow is not extended.

5.5 TDM/PCM Interface Timing

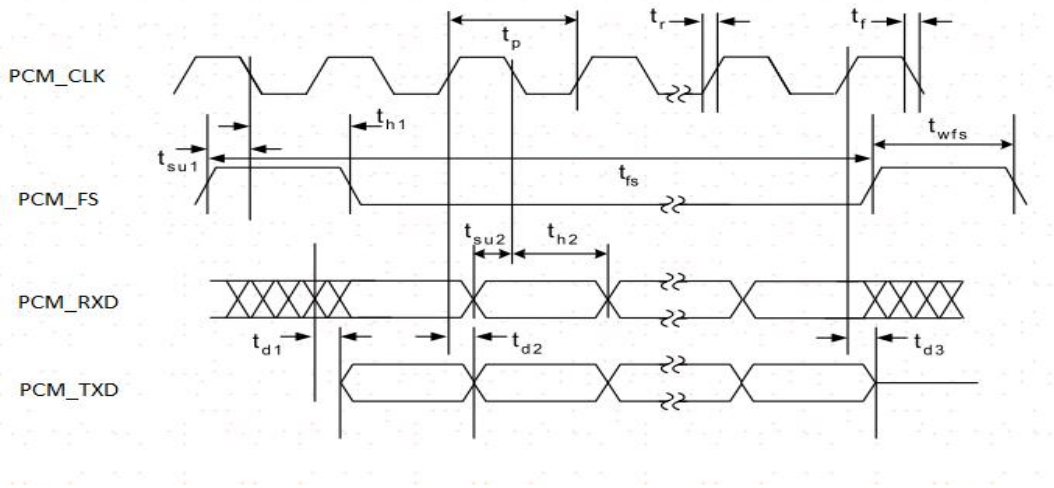


Figure 5-6 TDM/PCM Interface Timing

Table 5-5

Symbol	Parameter	Min.	Typ.	Max.	Units
tp	PCLK Period	--	2.048 4.096	--	Mhz
tfs	FSYNC Period		125		us
tsu1	Setup Time, FSYNC to PCLK Fall	25	--	--	ns
th1	Hold Time, FSYNC to PCLK Fal	20	--	--	ns
tsu2	Setup Time, DRX to PCLK Fall	25	--	--	ns
th2	Hold Time, DRX to PCLK Fall	20	--	--	ns

5.6 ISI Interface Timing

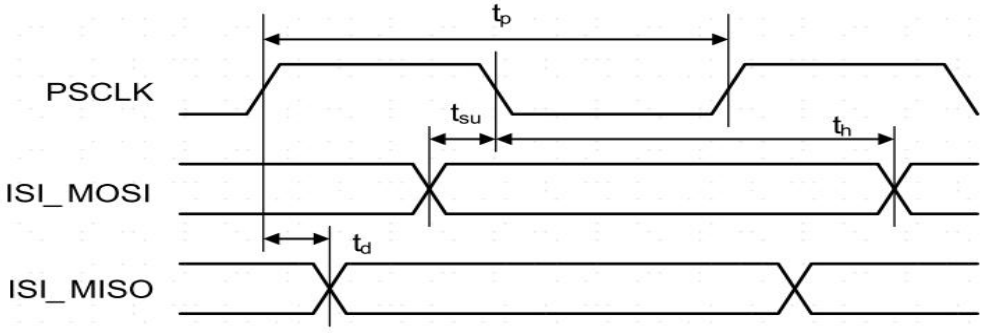


Figure 5-7 ISI Interface Timing

Table 5-6

Symbol	Parameter	Min.	Typ.	Max.	Units
tsu	Setup Time, ISI_MOSI to PSCLK Fall	7.5	--	--	ns

th	Hold Time, ISI_MOSI to PSCLK Fall	5	--	--	ns
td	Delay Time, PSCLK Rise to ISI_MISO	--		16	ns
tp	PSCLK Period	--	40.69	--	ns

5.7 SPI FLASH Interface Timing

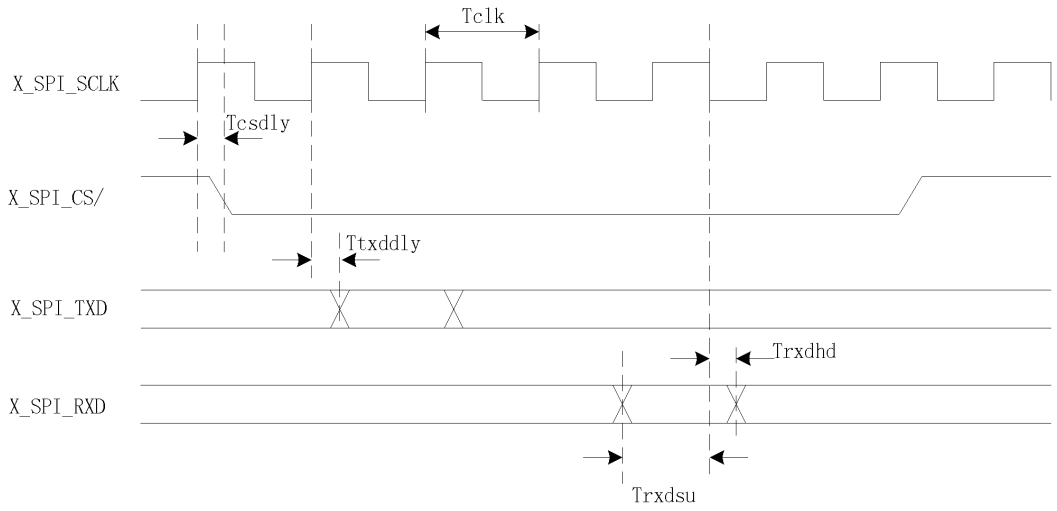


Figure 5-8 SPIFC Interface Timing

Table 5-7

Symbol	Parameter	Min.	Typ.	Max.	Units
X_SPI_SCLK clock cycle	Tclk	20	40	-	ns
Setup time for input	Trxdsu	10	-	-	ns
Hold time for input	Trxdhd	2	-	10	ns
Delay time for output @50Mhz,15pF	Ttxddly Tcsdly	-	-	8	ns

Note: The receiving direction uses the falling edge to sample the data.

5.8 NAND Interface Timing

Table 5-8 NAND AC Timing Characteristics for Command / Address / Data Input

Symbol	Parameter	Min.	Typ.	Max.	Units
tCLS	CLE setup time	12	-	-	ns
tCLH	CLE hold time	5	-	-	ns
tCS	-CE Setup time	20	-	-	ns
tCH	-CE hold time	5	-	-	ns

tWP	-WE pulse width	12	-	-	ns
tALS	ALE setup time	12	-	-	ns
tALH	ALE hold time	5	-	-	ns
tDS	Data setup time	12	-	-	ns
tDH	Data hold time	5	-	-	ns
tWC	Write cycle time	25	-	-	ns
tWH	-WE high hold time	10	-	-	ns
tADL	Addess to data loading time	100	-	-	ns

Table 5-9 AC Characteristics for Operation

Symbol	Parameter	Min.	Typ.	Max.	Units
tR	Data transfer from cell to register	-	-	25	us
tAR	ALE to -RE delay	10	-	-	ns
tCLR	CLE to -RE delay	10	-	-	ns
tRR	Ready to -RE low	20	-	-	ns
tRP	-RE pulse width	12	-	-	ns
tWB	-WE high to busy	-	-	100	ns
tWW	-WP low to -WE low	100	-	-	ns
tRC	Read cycle time	25	-	-	ns
tREA	-RE access time	-	-	20	ns
tCEA	-CE access time	-	-	25	ns
tRHZ	-RE high to output Hi-Z	-	-	100	ns
tCHZ	-CE high to output Hi-Z	-	-	30	ns
tCSD	-CE high to ALE or CLE don’t care	0	-	-	ns
tRHOH	-RE high to output hold	15	-	-	ns
tRLOH	-RE low to output hold	5	-	-	ns
tCOH	-CE high to output hold	15	-	-	ns
tREH	-RE high hold time	10	-	-	ns
tIR	Output hi-Z to -RE low	0	-	-	ns
tRHW	-RE high to -WE low	100	-	-	ns
tWHR	-WE high to -RE low	60	-	-	ns

5.9 USB2.0 Interface Characteristics

Table 5-10 USB2.0 Transmit DC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
High-speed Input Level						
Vhsdiff	High-speed deifferential input	|Vi(dp) - Vi(dm)|	300	-	-	mV

	sensitivity	Measured at the connecttion as an appplication circuit				
Vhscm	High-speed data signaling common-mode voltage range	-	-50	-	500	mV
Vhssq	High-speed squelch detechtion threshold	-	525	-	625	mV
High-speed Output Level						
Vhsoi	High-speed idle-level output voltage (differential)	-	-20	-	20	mV
Vhsol	High-speed low-level output voltage(differential)	-	-20	-	20	mV
Vhsoh	High-speed low-level output voltage(differential)	-	360	400	440	mV
Vchirpj	Chirp-J output voltage(differential voltage)	-	700	-	1100	mV
Vchirpk	Chirp-K output voltage(differential voltage)	-	-900	-	-500	mV
Idp/dm	Allowable output current of DP/DM lines	When the termination if 45Ω±10%	14.55	17.78	21.79	mA
High-speed Terminating Resistor						
Zhsdrv	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Zhsterm	Differential impedance	-	76.5	90	103.5	Ω

Table 5-11 USB2.0 AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
High-speed Drive Characteristics						
Thsdrat	High-speed TX data rate	-	479.76	-	480.24	Mbps

Thsdrat	High-speed RX data rate	-	479.76	-	480.24	Mbps
tHSR	High-speed differential rise time	10%~90%	100	-	-	ps
tHSF	High-speed differential fall time	10%~90%	100	-	-	ps
High-speed Drive Timing						
	Driver waveform requirement	Please refer to the eye pattern of template 1	Please follow template1 in the USB2.0 specification			
High-speed Receive Timing						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4	Please follow template4 in the USB2.0 specification			

Table 5-12 USB1.1 Transceiver DC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Input level for low-/full-speed						
Vih	High-level input voltage	driven	2.0	-	-	V
Vihz	High-level input voltage	floating	2.7	-	3.6	V
Vil	Low-level input voltage	-	-	-	0.8	V
Vdi	Differential input sensitivity	|Vi(dp) - Vi(dm)	0.2	-	-	V
Vcm	Differential common-mode voltage	Include Vdi range	0.8	-	2.5	V
Input levels for single-ended receiver						
Vse1	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels for low-/full-speed						
Vol	Low-level output voltage	-	0	-	0.3	V
Voh	High-level output voltage	-	2.8	-	3.6	V

Table 5-13 USB1.1 Transceiver AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Driver char for full-speed						
Tfdraths	Full-speed TX data rate	-	11.994	-	12.006	Mbps
Tfdraths	Full-speed RX data rate	-	11.994	-	12.006	Mbps
Driver char for low-speed						
Tldraths	low-speed TX data rate	-	1.49925	-	1.50075	Mbps
Tldraths	low-speed RX data rate	-	1.49925	-	1.50075	Mbps
Driving timing for full-speed						
	Propagation delay(VI,FSE0 OE to DP,DM)	-	-	-	15	ns
Tfdeop	Source jitter from differential transitions to SE0 transition	-	-2.0	-	5.0	ns
Tjr1	Receiver jitter	To the next transition	-18.5	-	18.5	ns
Tjr2	Receiver jitter	For the paired transition	-9.0	-	9.0	ns
Tfeopt	Source SE0 interval of EOP	-	160	-	175	ns
Tfeopr	receiver SE0 interval of EOP	-	82	-	-	ns
Tfst	Width of the SE0 interval during differential transition	-	-	-	14	ns
Driving timing for low-speed						
Tldeop	Source jitter from differential transition to SE0 transition	-	-40	-	100	ns
Tjr1	Receiver jitter	To next transition	-75	-	75	ns
Tjr2	Receiver jitter	For the paired transition	-45	-	45	ns
Tleopt	Source SE0 interval of EOP	-	1.25	-	1.5	us

5.10 USB3.0 Interface Characteristics

Table 5-14 USB3.0 Transmitter Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
UI	Units interval	-	199.94	200	200.06	ps
Vtx-diff-pp	Differential peak-to-peak TX voltage	2* |Vtxp - Vtxn|,measured at the TX near end	800	-	1200	mV
Vtx-diff-low	Low-power Differential peak-to-peak TX voltage	2* |Vtxp - Vtxn|,measured at the TX near end	400	-	1200	mV
Vtx-de-ratio	TX de-emphasis level	-	3.0	-	4.0	dB
Rtx-diff-dc	DC differentail impedance	-	75	-	200	Ω
Cac-coupling	AC Coupling capacitor	-	75	-	200	nF
Ttx-dj-far	Far-end TX deterministic jitter	Deterministic jtter assuming only the dual-dirac distribution	-	-	0.43	UI
Ttx-rj-far	Far-end TX random jitter	Measured at the TP1 and after receiver quualization function by using the CP1 pattern at 10^{-12} BER	-	-	0.23	UI
Ttx-tj-far	Far-end TX total jitter	Measured at the TP1 and after receiver equalization (Tj=Dj+Rj)	-	-	0.66	UI
Vtdr	The voltage change allowed during the reveiver detection	Total amount of the voltage change during TX-detect-RX	-	-	600	mV

Table 5-15 USB3.0 SSC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Tssc-mod-rate	Modulation rate	-	30	-	33	kHz
Tssc-freq-deviation	SSC deviation	-	+0/-4000	-	+0/-5000	ppm
Tssc-slew-rate	SSC slew rate	-	-	-	10	ms/s

Table 5-16 USB3.0 LFPS Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units

Tperiod	Period of the LFPS signal	-	20	-	100	ns
Vcm-ac-lfps	Ac common-mode voltage of the LFPS	-	-	-	100	mV
Vtx-diff-pp-lfps	Differential peak-to-peak LFPS voltage swing	2*|Vtxp-Vtxn|	800	-	1200	mV
Vtx-diff-pp-lfps-lp	Low-power differential peak-to-peak LFPS	2*|Vtxp-Vtxn|	400	-	600	mV
Trise-fall-2080	Rise/fall time of the LFPS signal	-	-	-	4.0	ns
Duty cycle	Duty cycle of the LFPS SIGNAL	-	40	-	60	%

Table 5-17 USB3.0 Receiver Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
UI	Units interval	-	199.94	200	200.06	ps
Rrx-dc	Receiver common-mode impedance	-	18	-	30	Ω
Rrx-diff-dc	Receiver DC differential impedance	-	72	-	120	Ω
Vrx-lfpsdet-diff-pp	LFPS detect threshold	-	100-		300	mV

Table 5-18 USB3.0 RX Input Jitter Tolerance

Symbol	Description	Condition	Min.	Typ.	Max.	Units
F1	Tolerance corner	-	-	4.9	-	MHz
Jrj	Random jitter	-	-	0.0121	-	UI rms
Jrj_p-p	Random jitter peak-to-peak at 10^{-12}	-	-	0.17	-	UIp-p
Jpj_500khz	Sinusoidal jitter	-	-	2.0	-	UIp-p
Jpj_1mhz	Sinusoidal jitter	-	-	1.0	-	UIp-p
Jpj_2mhz	Sinusoidal jitter	-	-	0.5	-	UIp-p
Jpj_f1	Sinusoidal jitter	-	-	0.2	-	UIp-p
Jpj_50mhz	Sinusoidal jitter	-	-	0.2	-	UIp-p

5.11 DDR Interface Characteristics

Table 5-19 DDR Interface Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unitss
Voh	DC output high	-	0.80* VDDQ for DDR3	-	-	V

Vol	DC output low	-	-	-	0.20 * VDDQ for DDR3	V
ODT	120,60,40 ohms	-	-10	typ	+10	-
Ron	34.0/40.0/48.0 ohms	-	-12	typ	+12	%
Ioz	Output leakage current	-	-5	-	+5	uA
Vihdq(AC)	AC input high	-	Vref+0.175	-		V
Vildq(AC)	AC input low	-	-	-	Vref-0.175	V
Vihdq(DC)	DC input high	-	Vref+0.1	-	VDD	V
Vildq(DC)	DC input low	-	VSS	-	Vref-0.1	V
Vrefdq	ODT enable	-	-	0.5 * Vddq for DDR3 and middle of pad voltage for DDR4	-	V

5.12 Serdes Interface Characteristics

5.12.1 Receive Direction Characteristics

Table 5-20 Receive Input Eye Diagram Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
V RX-DIFF-PKPK	Receiver input differential peak-to-peak voltage	Closed eye	-	**2000**	mV diff-pkpk
V RX-CM-DC	Receiver input DC common-mode voltage	-	0	-	mV
V RX-CM-AC	Receiver Input AC common-mode voltage	-150	-	150	mV pkpk
T RX-DDJ	Receive input signal data dependent Jitter (Inter-symbol interference)	-	-	1	UI pkpk
T RX-RJ	Receive input random jitter	-	-	0.3	UI pkpk
T RX-PJ	Receive input period jitter (At high frequency)	-	-	0.1	UI pkpk
T RX-TJ	Receive input Total Jitter (DDJ + RJ + PJ).	-	-	1	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-pass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to	-	1667	-	F BAUD /F GPLL

	the data rate				

Table 5-21 Receive Loop Loss

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Receiver differential DC return loss	-	-	-20	dB
Z RL-DIFF-NYQ	Receiver differential return loss at 5.0 GHz	-	-	-2.5	dB
Z RL-CM-DC	Receiver common-mode DC return loss	-	-	-10	dB
Z RL-CM-NYQ	Receiver common-mode return loss at 5.0 GHz	-	-	-5	dB

Table 5-22 Receive DC Resistance

Parameter	Description	Min.	Typ.	Max.	Units
R DIFF-DC	DC differential receive impedance	80	100	110	Ω
R CM-DC	DC common-mode receive impedance	20	25	27.5	Ω
R DIFF-HIZ-POS	Differential receive high-impedance for input voltage from 0 V to 200 mV	200k	-	-	Ω
R CM-HIZ-POS	Common-mode receive high-impedance for input voltage from 0 V to 200 mV	20k	-	-	Ω
R DIFF-HIZ-NEG	Differential receive high-impedance for input voltage from -150 mV to 0 mV	4k	-	-	Ω
R CM-HIZ-NEG	Common-mode receive high-impedance for input voltage from -150 mV to 0 mV	1k	-	-	Ω

Table 5-23 Received Signal Detection

Parameter	Description	Min.	Typ.	Max.	Units
V IDLE-THRESH	Receiver signal detect input voltage threshold	75	120	175	mV diff-pkpk
T SIGDET-ATTACK	Signal detect valid signal attack time (Turn-on time) in SATA mode	-	-	15	ns
T SIGDET-DECAY	Signal detect valid signal decay time (Turn-off time) in SATA mode	-	-	15	ns
T SIGDET-ATT-DECAYMIS	Signal detect attack/decay time mismatch in SATA mode	-	-	5	ns

5.12.2 Transmit Direction Characteristics

Table 5-24 Output Eye Diagram Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
V TX-DIFF-PKPK	Backporch transmit amplitude	400	-	1400	mV diff-pkpk
V TX-EYE-PKPK	Transmit eye voltage opening	400	-	1200	mV diff-pkpk

D TX-N+1-DEEMP	N+1 precursor tap De-emphasis	0	-	5.0	dB
D TX-N-1-DEEMP	N-1 postcursor tap De-emphasis	0	-	8.5	dB
D TX-N-2-DEEMP	N-2 postcursor tap De-emphasis	0	-	2.0	dB
T TX-SLEW	Rise/Fall time	30	-	120	ps
T TX-PJ	Transmit periodic jitter Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	0.05	UI pkpk
T TX-RJ	Transmit total peak-to-peak random jitter (Assumes 14 TXRJ-RMS) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	0.15	UI pkpk
T TX-TJ	Transmit total peak-to-peak jitter (Assumes T TX - TJ = T TX-DDJ + T TX-PJ + T TX-RJ) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	0.25	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-sass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to the data rate	-	1667	-	F BAUD / F GPLL
V TX-CM-PKPK-AC	AC common-mode voltage variation (Peak-to- peak) at PCIe Gen2 rate	-	-	100	mV
V TX-CM-RMS-AC	AC common-mode voltage variation (RMS) at PCIe Gen1 rate	-	-	20	mV

Table 5-25 Transmitter DC Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
Z TX-DIFF-DC	Transmitter output differential DC impedance	80	100	120	Ω
Z TX-CM-DC	Transmitter output common-mode DC impedance	20	25	30	Ω
Z TX-DIFF-HIZ	Transmitter output differential DC impedance in squelch mode	-	-	>2k	Ω
Z TX-CM-HIZ	Transmitter output common-mode DC	-	-	> 500	Ω

	impedance in squelch mode				

Table 5-26 Transmitter Loop Loss

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Transmitter differential DC return loss	-	-	-20	dB
Z RL-DIFF-NYQ	Transmitter differential return loss at 5.0 GHz	-	-	-4	dB
Z RL-CM-DC	Transmitter common-mode DC return loss	-	-	-10	dB
Z RL-CM-NYQ	Transmitter common-mode return loss at 5.0 GHz	-	-	-5	dB

Table 5-27 Idle Condition

Parameter	Description	Min.	Typ.	Max.	Units
V TX-IDLE	Idle output voltage	-	-	20	mV pkpk
V CM-DELTA-SQUELCH	Maximum common-mode step entering/exiting squelch mode	-	-	50	mV
T TX-IDLE-LATENCY	Latency entering/exiting idle	-	-	8	ns

Table 5-28 Receive Detection

Parameter	Description	Min.	Typ.	Max.	Units
V TX-RCV-DETECT	Voltage change allowed during receiver detection	-	-	600	mV

5.13 GEPHY Interface Characteristics

Table 5-29 AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
AC Characteristics						
-	Reference frequency	-	25-0.005%	25	25+0.005%	MHz
-	Reference clock duty cycle	-	40	50	60	%
I_ASICIN_OBD jitter1	Period jitter of the clock from ASIC instead of from external crystal	-	-	-	80	ps
I_ASICIN_OBD jitter2	Cycle-to-cycle jitter of the clock from ASIC instead of from external crystal	-	-	-	120	ps
I_ASICIN_OBD jitter3	Long-term jitter of the clock from ASIC instead of from external crystal (set the trigger delay to 10us)	-	-	-	160	ps
Transmitter char						
2 x Vtxa	Peak-to-peak differential	10BASE-Te	3.08	3.5	3.92	V

	output voltage	mode				
2 x Vtxa	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2.0	2.1	V
2 x Vtxa	Peak-to-peak differential output voltage	1000BASE-T mode	-	2.0	-	V
Tr/Tf	Signal rise/fall time	100BASE-TX mode	3.0	4.0	5.0	ns
-	Output jitter	100BASE-TX mode Scrambled idle signal	-	-	1.4	ns
Vtxa	Overshoot	100BASE-TX mode	-	-	5.0	%
Receiver char						
-	Error-free cable length	-	100	-	-	meter

5.14 PCIE2.0 Interface Characteristics

Table 5-30 PCIE Interface Signal Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
VIN	Differential input voltage	120	-	**1000**	mVpdd
VRIN	Differential input impedance	80	100	**120**	Ω
VOD	Differential output voltage	800	-	**1200**	mVpdd
VROUT	Differential output impedance	80	100	**120**	Ω

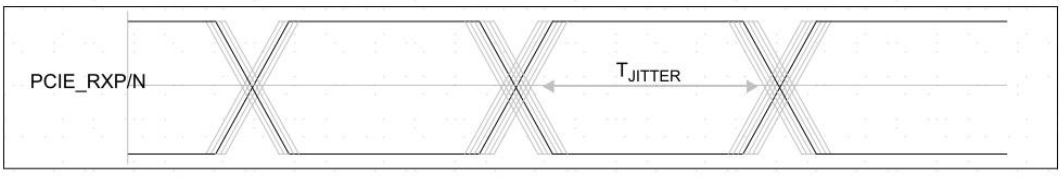


Figure 5-9 PCIE RX Timing

Table 5-31 RX Receive Characteristic

Parameter	Description	Min.	Typ.	Max.	Units
FREQ	Baud Rate	-	2.5/5.0	-	Gbaud
RIN	Input Impedance (Differential)	80	100	120	Ω
VID	Input Voltage (Differential pk-pk)	120	-	1000	mVp-p
TJ	Jitter Tolerance (Min Rx EYE width)	0.4	-	-	Ω

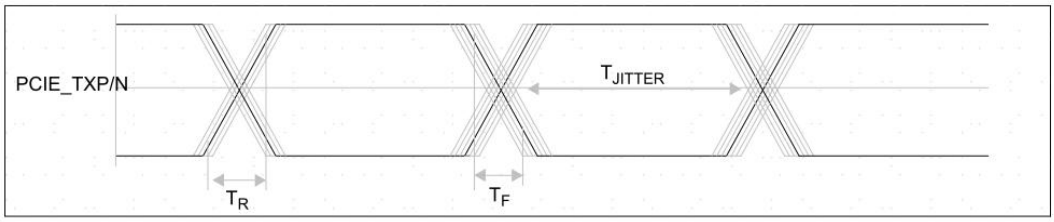


Figure 5-10 PCIE TX Timing

Table 5-32 RX Transmitter Characteristic

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FREQ	Baud Rate			2.5/5.0	-	Gbaud
ROUT	Output Impedance (Differential)		80	100	120	Ω
VOD	Output Voltage (Differential pk-pk)		800	1000	1200	mVp-p
TR/TF	Output Rise/Fall Time (20%~80%)		0.125	-	-	UI
VOEQ	Output De-Emphasis	Gen1 2.5 Gbps Gen2 5.0 Gbps	-3.0 -5.5	-3.5 -6.0	-4.0 -6.5	dB
TR/TF	Rise/Fall Time (20%–80%)	Gen1 2.5 Gbps Gen2 5.0 Gbps	0.125 0.150	- -	- -	ns
TJ	Jitter (min Tx EYE width)		0.75	-	-	UI

5.15 100Mhz Differential IO Characteristics

Table 5-33 100Mhz Differential IO Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
|Vdiff.pp|	Differential CML ouput voltage (peak to peak)	-	600	-	1100	mV
Voc	Output common-mode	-	250	-	550	mV
Tr,diff	Differential CML output rise time(30%~70%)	Load=1pF	-	-	500	ps
Tf,diff	Differential CML output fall time(70%~30%)	Load=1pF	-	-	500	ps
Tr,single	Sing-ended buffer output rise time(30%~70%)	Load=100fF	-	-	150	ps
Tf,single	Sing-ended buffer output fall time(70%~30%)	Load=100fF	-	-	150	ps
Ddiff	Differential CML output duty cycle	Load=1pF	47.5	-	52.5	%

JT	Differential CML output toal additive jitter	Load=1pF Without power noise	-	-	6.00	ps
	Differential CML output toal additive jitter	Load=1pF With power noise	-	-	55.0	ps
C_{AC}	AC-coupled capacitor	-	100	-	-	nF
R_L	Differential CML output termination resistance	-	-	100	-	Ω
Tsettle	Settle time	-	-	-	10	us

Power noise requirements/limitation:

1. HF(~100MHz):Typical resonance frequency at package +on-die power delivery,known at the 1st droop (Amp:35mVpp)
2. MF(~3MHz):Typical 2nd droop drequency.(Amp :10mVpp)
3. LF(100KHz):Typical 3rd droop frequency. From VR/Boad loop(Amp:5mVpp)

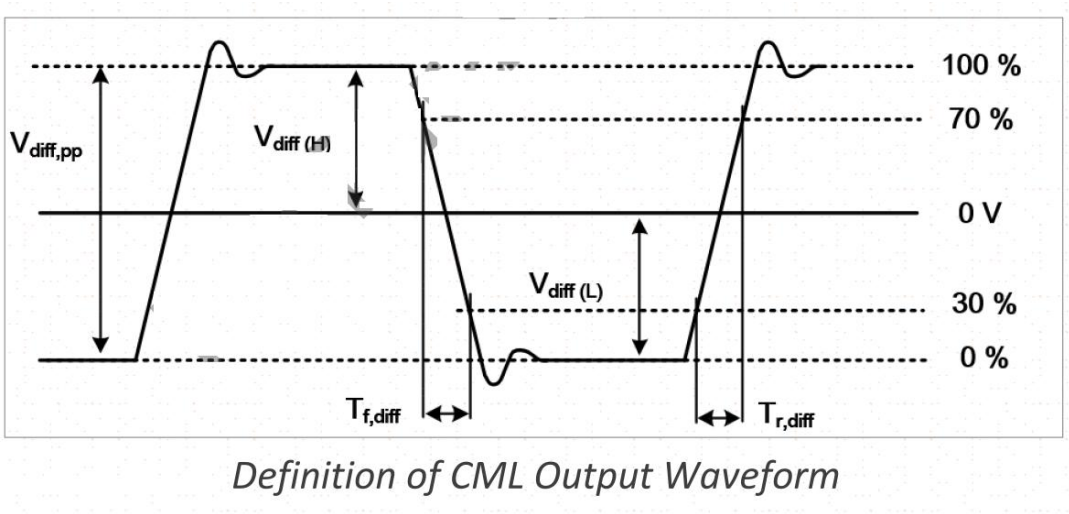


Figure 5-11 Definition of CML output waveform

6 Clock Input Requirements

The chip requires an external input of 25Mhz clock. Passive crystal oscillator circuit or active crystal oscillator can be used. The input 25MHz clock has the following requirements:

Table 6-1

Symbol	Description	Min.	Typ.	Max.	Units

VIH	Input high voltage	2.0	--	--	V
VIL	Input low voltage			0.8	V
Tfrequency	Clock frequency		25		MHz
Δfrequency	Clock tolerance	-50	-	50	ppm
C1	Load cap	12		27	pF
C2	Load cap	12		27	pF
Tdc	Duty cycle		50%		%

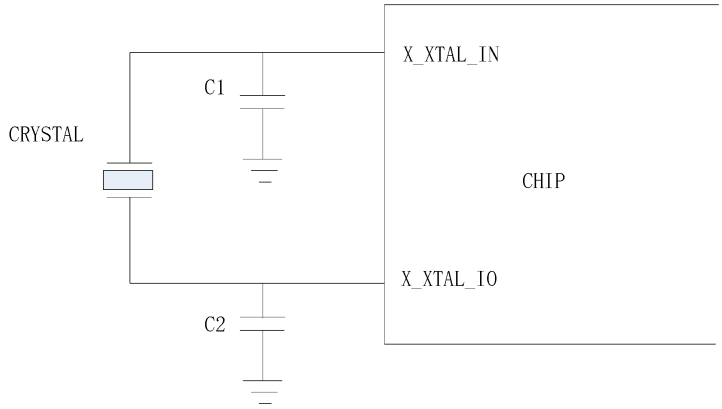


Figure 6-1 Crystal Circuit Diagram

7 Reliability Characteristics

7.1 Reliability Parameters

Table 7-1

Parameter	Max.	Units	Notes
HBM	2K	V	
CDM	250	V	
MM	200	V	
Latch-up	200	mA	
MSL	3	Grade	

7.2 Maximum Working Environment

Table 7-2

Parameter	Symbol	Min.	Max.	Units
Junction temperature limit	Tj	-40	+125	℃

7.3 Recommended Working Environment

Table 7-3

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient temperature	Ta	0	25	70	℃
Welding temperature	Tp	225	235	245	℃
Junction temperature	Tj	-40	-	125	℃
Storage temperature	Ts	-55	-	150	℃
Relative humidity	RH	-	50	90	%

7.4 Thermal Characteristics

Table 7-4 Thermal Resistance

Theta Ja (˚C/W)			Psi jt (˚C/W)	Theta Jc (˚C/W)	Theta Jb (˚C/W)
0 m/s	1 m/s	2 m/s			
29	23.7	22.5	0.27	9.5	12.38

8 Power Parameters

8.1 Power Consumption

Maximum Power Consumption: 4.50W（Environmental: 70° C）

Typical Power Consumption: 3.70W（Environmental: 25° C）

8.2 MAX current of power branch

Table 8-1

Name	Num	Voltage Value (V)	Range	Noise Tolerance (mV)	MAX Current (mA)	Notes

VCC3IO	12	3.3	±10%	30	260	3.3V IO digital power
VCC3IO_OSC	1	3.3	±10%	30	3	3.3V OSC digital power
VCC33A_GPHY	3	3.3	-5%~+10%	30	329	GPHY 3.3V analog power
VCC120_DDR	12	1.2/1.5	-5%~+10%	30	450	DDR3/DDR4 PHY IO power: DDR3: connect to 1.5V DDR4: connect to 1.2V
VCC12O_DDRCK	4	1.2/1.5	-5%~+10%	30		DDR3/DDR4 PHY CK IO power: DDR3: connect to 1.5V DDR4: connect to 1.2V
VCC18A_DDR_PLL	1	1.8	-5%~+10%	30	7	1.8V DDRPHY PLL analog power
VCC09K_DDR_PHY	8	0.9	-5%~+10%	30	198	DDRPHY 0.9V digital power
VCC11K	10	1.1	±10%	30	350	GPHY 1.1V core digital power
VCC11A_GPHY	3	1.1	-5%~+10%	30	450	GPHY 1.1V analog power
VCCK	26	0.9	±10%	30	1200	0.9V core digital power
VCC18UPS	6	1.8	±10%	30	300	Multi-Voltage IO 1.8V digital power
VCC18IO	2	1.8	±10%	30		1.8V IO digital power
VCC18IO_OSC	1	1.8	±10%	30	2	1.8V OSC digital power
VCC09A_PON	2	0.9	-5%~+10%	30	80	0.9V PON analog power
VCC09A_AUX_PON	1	0.9	-5%~+10%	30		0.9V serdes auxiliary analog power
VCC09A_ETH	2	0.9	-5%~+10%	30	80	0.9V ETH analog power
VCC09A_AUX_ETH	1	0.9	-5%~+10%	30		0.9V serdes auxiliary analog power
VCC_VPH	1	1.8	-5%~+10%	30	70	1.8V PCIePHY analog power
VCC_VP	1	0.9	-5%~+10%	30	120	0.9V PCIePHY analog power
VCC_VPTX0_P0	1	0.9	-5%~+10%	30		0.9V PCIePHY analog transmit power
VCC_VPTX0_P1	1	0.9	-5%~+10%	30		0.9V PCIePHY analog transmit power
VCC09A_LVTX	1	0.9	-5%~+10%	30	5	0.9V differential IO analog power
VCC09A_PLL_BUS	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09A_PLL_CPU	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09A_RX_USB3	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09A_TX_USB3	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09P_U_PLL_DDR	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09P_U_PLL_ETH	1	0.9	-5%~+10%	30	5	0.9V PLL analog power
VCC09P_U_PLL_PON	1	0.9	-5%~+10%	30	5	0.9V PLL analog power
VCC09P_U_PLL_SYNC	1	0.9	-5%~+10%	30	3	0.9V PLL analog power

VCC09P_U_PLL_TDM	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC09P_U_PLL_USB	1	0.9	-5%~+10%	30	3	0.9V PLL analog power
VCC18A_ETH	1	1.8	-5%~+10%	30	70	1.8V serdes analog power
VCC18A_PON	1	1.8	-5%~+10%	30	70	1.8V serdes analog power
VCC18A_TDC	1	1.8	-5%~+10%	30	2	1.8V TDC analog power
VCC18A_U_PLL_DDR	1	1.8	-5%~+10%	30	5	1.8V PLL analog power
VCC18A_U_PLL_ETH	1	1.8	-5%~+10%	30	15	1.8V PLL analog power
VCC18A_U_PLL_PON	1	1.8	-5%~+10%	30	15	1.8V PLL analog power
VCC18A_U_PLL_SYNC	1	1.8	-5%~+10%	30	5	1.8V PLL analog power
VCC18A_U_PLL_TDM	1	1.8	-5%~+10%	30	5	1.8V PLL analog power
VCC18A_U_PLL_USB	1	1.8	-5%~+10%	30	5	1.8V PLL analog power
VCC18A_USB2	1	1.8	-5%~+10%	30	40	1.8V USB2.0PHY analog power
VCC18A_USB3	1	1.8	-5%~+10%	30	59	1.8V USB3.0PHY analog power
VCC18A_VDT	1	1.8	-5%~+10%	30	2	1.8V VDT analog power
VCC33A_USB2	1	3.3	-5%~+10%	30	10	3.3V USB2.0PHY analog power
VCC33A_USB3	1	3.3	-5%~+10%	30	10	3.3V USB3.0PHY analog power

8.3 Power on and Power off sequence

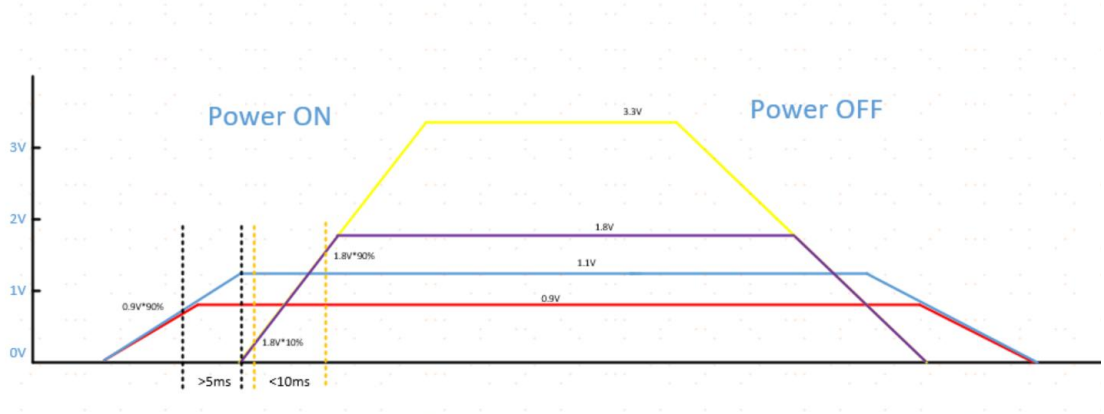


Figure 8-1 Chip Power-on Sequence Diagram

The chip is powered on and powered off according to the following recommended sequence:

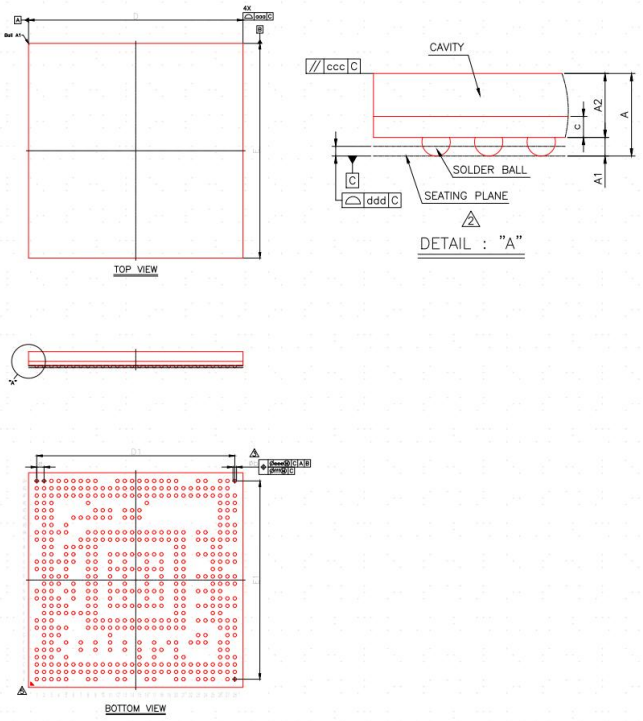
1. Power on 0.9V and 1.1V first, and keep 0.9V for more than 5ms before powering on 1.8 and 3.3V;
2. 0.9V and 1.1V can be powered on at the same time;
3. 1.8V and 3.3V can be powered on at the same time;
4. The 1.8V power-on time should be less than 10ms;
5. Power off 1.8V and 3.3V first, and power off after 0.9V and 1.1V.

8.4 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
I/O ring supply (3.3V) and Analog, reference	VCC3IO,VCC33A (Including all 3.3V supply)	-0.5	4.6	V
I/O ring supply (1.8V) and Analog, reference	VCC18, VCC18A (Including all 1.8V supply)	-0.5	2.5	V
DDR I/O ring supply(1.5V)	VDDQ	-0.4	1.98	V
Analog and digital core logic supply(0.9V)	VCC, VCCK (Including all 0.9V supply)	-0.4	1.05	V
I/O ring supply (1.1V) and Analog, reference	VCC11K, VCC11A (Including all 1.1V supply)	-0.5	1.5	V

9 Mechanical Characteristics

Packaging Characteristics



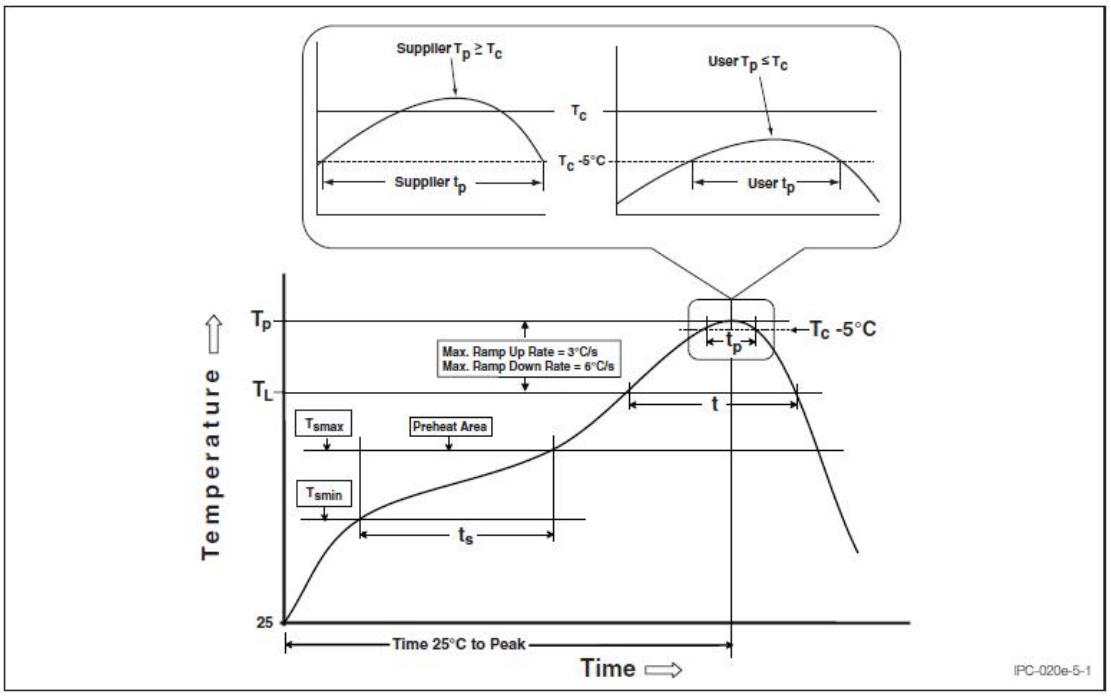
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.36	1.43	1.50	0.054	0.056	0.059
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	1.17	1.22	1.27	0.046	0.048	0.050
c	0.32	0.36	0.40	0.013	0.014	0.016
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.55	---	---	0.691	---
E1	---	17.55	---	---	0.691	---
e	---	0.65	---	---	0.026	---
b	0.26	0.31	0.36	0.010	0.012	0.014
aaa		0.15			0.006	
ccc		0.20			0.008	
ddd		0.15			0.006	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME	28/28					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.30 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

Figure 9-1 Packaging Physical Dimensions

10 Reflow Profile



Profile	**Sn-Pb Eutectic Assembly**	**Pb-Free Assembly**
Preheat and soak Min. temperature (Ts_{min}) Max. temperature (Ts_{max}) Time (ts_{min} to ts_{max}) (t_s)	 100 °C 150 °C 60 ~ 120 seconds	 150 °C 200 °C 60 ~ 120 seconds
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second (Max.)	3 °C/second (Max.)
Liquid temperature (T_L) Time at liquid (t_L)	183 °C 60 ~ 150 seconds	217 °C 60 ~ 150 seconds
Peak package body temperature (T_p)*	235℃	260℃
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to Ts_{max})	6 °C/second (Max.)	6 °C/second (Max.)
Time to peak temperature from 25 °C	6 minutes (Max.)	8 minutes (Max.)
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		