5VT2518
DATASHEET

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REVISION HISTORY

Revision	Release Date	Author	Change	Remark
V1.0	2021/9/30	Wingston	Initial version	
V1.1	2022/8/11	Wingston	English version	
	2022/9/22	Wingston	Update BALLMAP,Modify PIN default NAME and Description	
	2022/12/13	Wingston	Add Absolute maximum rating	

1 General Description

1.1 Chip Introduction

5VT2518 is an optical modem + switching chip with built-in multi-core processor, supporting GPON and EPON fiber access, as well as Layer 2 switching and Layer 3/4 hardware NAT/NAPT functions as a SOC chip; Equipped with 4 Ethernet ports, supports DDR3/DDR4 particles, supports plug-in WIFI chip through PCIE interface to achieve WIFI access, realizing the function of low-cost home optical modem and gateway in one. The chip supports Layer 2 and supports Layer 3 NAT/NAPT hardwired network switching. The chip can be used for a variety of service applications on the upper layer of the processor, such as DHCP, HTTP and some services that require the use of hardwired forwarding functions.

The chip has an integrated GPON and EPON engine to support network bridging and routing services for handling ultra-low cost optical network terminals. The chip has built-in powerful protocol analysis functions and can handle various hard forwarding services such as VLAN, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP messages. For VLAN and PPPoE protocols, the chip supports automatic encapsulation and decapsulation of VLAN tagged frames and PPPoE headers. The chip supports port-based, protocol-based, VLAN-based, etc. It supports up to 4,000 VLAN groups and supports the SPAN tree protocol, whose states can be divided into four: forbidden, blocking, listening and forwarding.

Features

- System Processor
  Multi-core processor
  L2 Cache: 256KB
- Flash Interface
  SPI NAND Flash, SPI NOR Flash, Maximum capacity 32Gb
  Parallel NAND flash, Maximum capacity 32Gb
- Supports 4-port GEPHY
- Supports DDR3/DDR4
  16-bits DDR3/DDR4
  Supports the highest rate of 1600Mbps
  Maximum capacity 8Gb (1GB)
- 1 USB2.0 interface, Host mode
- 1 USB3.0 interface, Host mode
- 2 PCIE2.0 interfaces, RC mode
- 1 TDM interface, supports TDM+SPI mode
  2 VoIP interface
- 1 ISI interface, 2 VoIP interface
- I2C interface

Supports 2 I2C interface, 7bit/10bit address mode

- UART interface

Supports compatible 16550 UART interface

3 UART interfaces, 1 of which can be multiplexed

- 1 SPI interface
- 1 MDIO interface
- 1 RGMII interface
- GPON

Compliant with ITU G.984.x protocol standard

Supports data rates of 1.24416G upstream/2.48832G downstream

Supports 32 TCONT, 320 GEM

Supports AES, key switching

Supports uplink and downlink FEC

Supports DBRu reporting

Hardware dying gasp

- EPON

Compliant with 802.3 EPON MAC standard

8 independent LLIDs

Supports data rates of 1.25G upstream/1.25G downstream

Supports DS/US FEC

Supports downlink service encryption

Supports US scheduling

Supports queue rate control setting (CIR/PIR)

Supports strict priority and weighted fair queuing modes

Supports RC4837 Counter

Hardware dying gasp

- Layer 2/layer 3 packet hardware accelerator for NAT/NAPT

Supports 32K NAPT rules /4K NAPTR rules

Supports based on port/VLAN binding

Supports IPv4/IPv6 protocols

Supports IPoE/DHCP/PPPoE/DS-Lite WAN hardware packet accelerator

Supports DS-Lite multicast

Supports VxLAN hardware forwarding

Supports NAPTv6 hardware forwarding

- L2 capability

Supports 4 Gigabit Ethernet ports

Supports non-blocking wire-speed receiving and sending and non-head-of-line blocking/forwarding

Embedded 512 entry 4-way hash L2 lookup table

Supports source and destination MAC address filtering

- Supports ACL

Based on MAC, IP, TCP/UDP, ICMP,IGMP, IPv6

Supports actions of mirror, redirect, dropping

Supports queuing and scheduling, traffic monitoring

CVLAN decision, SVLAN designation

Supports packet length/VID/IP/L4 Port range check

- 16 PON classification rules
  Supports SVLAN tagging/removing
  Supports CVLAN tagging/removing
  Supports indirect LLID/GEMPort specification
  Supports forced UNI port forwarding and queue priority designation
- IEEE 802.1Q VLAN
  Supports 4K VLAN
  Supports Untag definition in each VLAN
  Supports VLAN based on port and protocol
- Supports IEEE 802.1ad Stacking VLAN
- Supports 2 users to define TPID
- Supports IVL, SVL, and IVL/SVL
- Supports 512 MAC address table, 4 hash calculation
- Supports Spanning Tree
- Supports IEEE 802.3x full-duplex and half-duplex flow control mechanism
- Supports IEEE 802.1X access control protocol
- Supports Quality of Service (QoS)
- Supports strict priority and weighted fair queuing modes
- Supports port to monitoring destination port
- Supports OAM
- Supports IGMP/MLD trap detection function
- Supports to prevent DOS attack
- Supports 25mhz single-end crystal input or crystal oscillator input
- BGA-410 17x17mm package

1.2 Block Diagram

The connection relationship of the chip in the application as below:

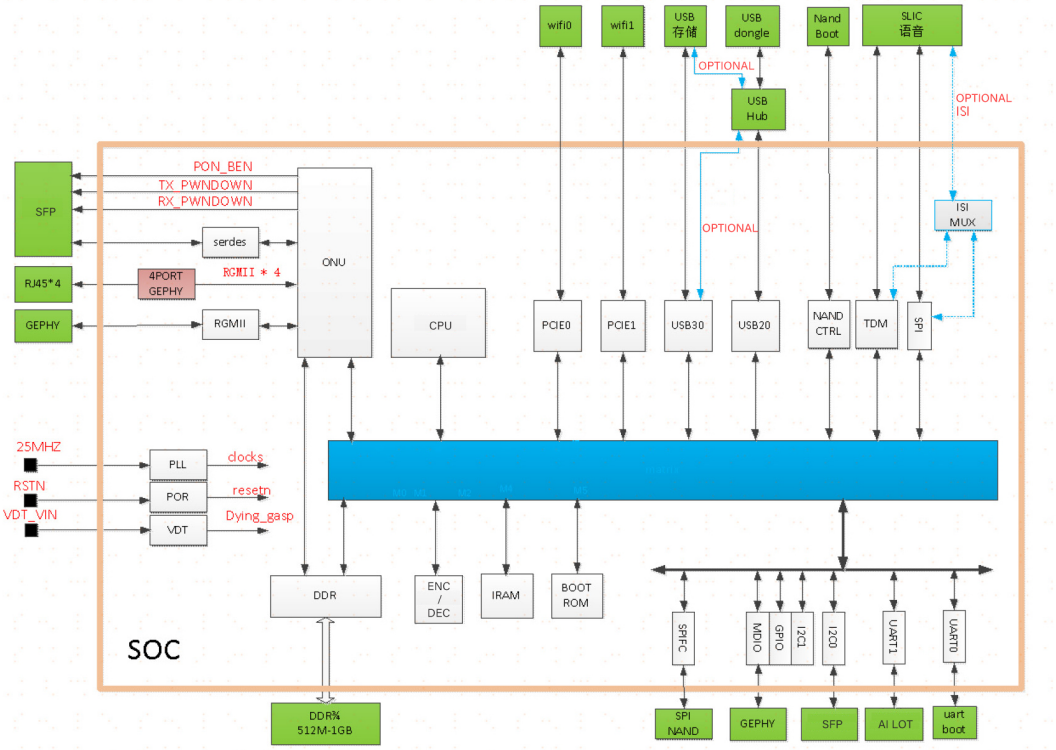


Figure1-1 Block Diagram

2 Balls

2.1 Ball map

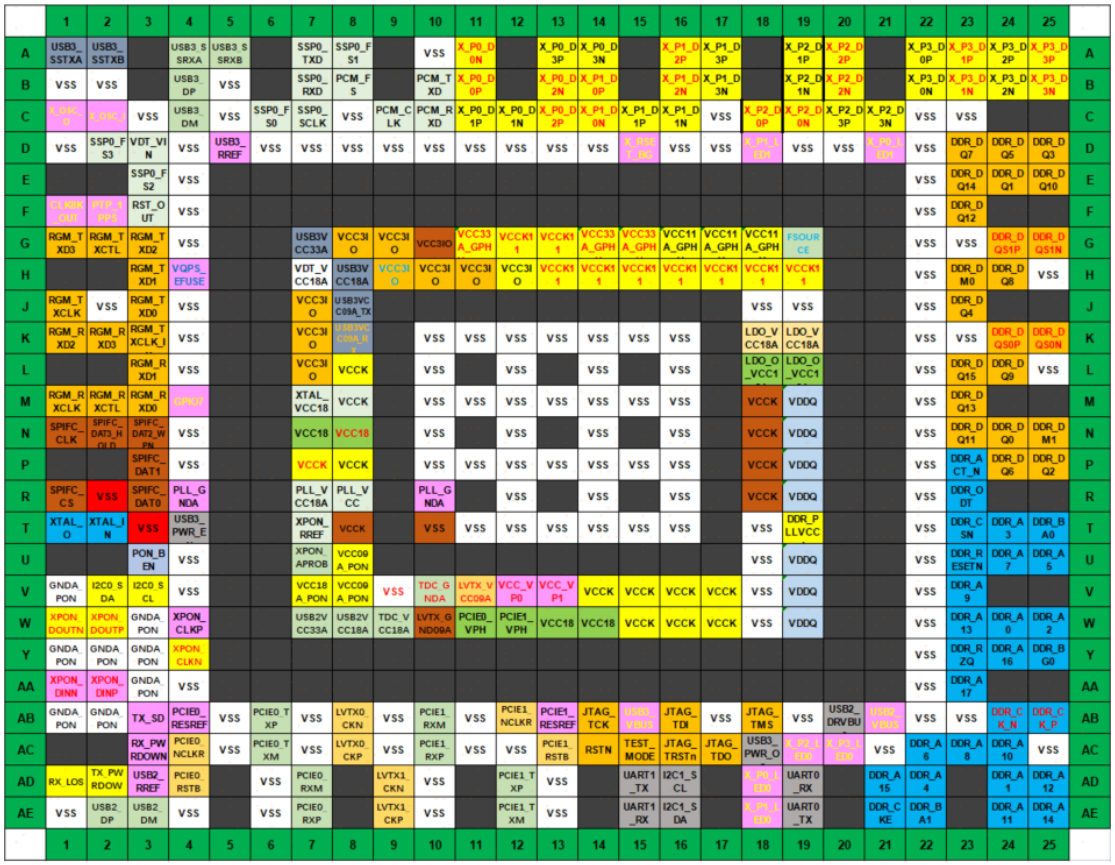


Figure 2-1 5VT2518 Ball Map

2.2 Balls Description

AI ： Analog input

AIO ： Analog input/output

AO ： Analog output

IT ： Input, TTL compatible

OT ： Tristate output, TTL compatible

ITOT： Input/Output, TTL compatible

SSTL_O：SSTL interface standard output

SSTL_B：SSTL interface standard input/Output

PG ： Power Ground

Table 2-1 MDI Interface Pins

Pin No.	Name	IO Type	Default Value	Description
A11	X_P0_D0N	AIO	Bidirectional Differential IO	MDI[0], Port0. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
B11	X_P0_D0P	AIO	Bidirectional Differential IO	
C12	X_P0_D1N	AIO	Bidirectional Differential IO	MDI[1], Port0. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
C11	X_P0_D1P	AIO	Bidirectional Differential IO	
B13	X_P0_D2N	AIO	Bidirectional Differential IO	MDI[2], Port0. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
C13	X_P0_D2P	AIO	Bidirectional Differential IO	
A14	X_P0_D3N	AIO	Bidirectional Differential IO	MDI[3], Port0. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A13	X_P0_D3P	AIO	Bidirectional Differential IO	
C14	X_P1_D0N	AIO	Bidirectional Differential IO	MDI[0], Port1. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
B14	X_P1_D0P	AIO	Bidirectional Differential IO	
C16	X_P1_D1N	AIO	Bidirectional Differential IO	MDI[1], Port1. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
C15	X_P1_D1P	AIO	Bidirectional Differential IO	
B16	X_P1_D2N	AIO	Bidirectional Differential IO	MDI[2], Port1. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A16	X_P1_D2P	AIO	Bidirectional Differential IO	
B17	X_P1_D3N	AIO	Bidirectional Differential IO	MDI[3], Port1. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A17	X_P1_D3P	AIO	Bidirectional Differential IO	
C19	X_P2_D0N	AIO	Bidirectional Differential IO	MDI[0], Port2. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
C18	X_P2_D0P	AIO	Bidirectional Differential IO	
B19	X_P2_D1N	AIO	Bidirectional Differential IO	MDI[1], Port2. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
A19	X_P2_D1P	AIO	Bidirectional Differential IO	
B20	X_P2_D2N	AIO	Bidirectional	MDI[2], Port2. BI_DC± and MDIX mode in 1000Base-T MDI

			Differential IO	mode are equivalent to BI_DD±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A20	X_P2_D2P	AIO	Bidirectional Differential IO	
C21	X_P2_D3N	AIO	Bidirectional Differential IO	MDI[3], Port2. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
C20	X_P2_D3P	AIO	Bidirectional Differential IO	
B22	X_P3_D0N	AIO	Bidirectional Differential IO	MDI[0], Port3. BI_DA± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DB±; 100Base-TX and 10Base-Te MDI modes are sending, and MDIX is receiving.
A22	X_P3_D0P	AIO	Bidirectional Differential IO	
B23	X_P3_D1N	AIO	Bidirectional Differential IO	MDI[1], Port3. BI_DB± and MDIX modes of 1000Base-T MDI mode are equivalent to BI_DA±; 100Base-TX and 10Base-Te MDI modes are receiving, and MDIX is sending.
A23	X_P3_D1P	AIO	Bidirectional Differential IO	
B24	X_P3_D2N	AIO	Bidirectional Differential IO	MDI[2], Port3. BI_DC± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DD±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A24	X_P3_D2P	AIO	Bidirectional Differential IO	
B25	X_P3_D3N	AIO	Bidirectional Differential IO	MDI[3], Port3. BI_DD± and MDIX mode in 1000Base-T MDI mode are equivalent to BI_DC±; 100Base-TX and 10Base-Te mode can be left floating when not in use.
A25	X_P3_D3P	AIO	Bidirectional Differential IO	
D15	X_RSET_BG	AIO	Bidirectional Differential IO	Reference resistor pin, external 3kohm±1% to GND

Table 2-2 DDR Interface Pins

Pin No.	Name	IO Type	Default Value	Description
W24	DDR_A0	SSTL_O	DDR Analog IO	DDR Address
AD24	DDR_A1	SSTL_O	DDR Analog IO	DDR Address
W25	DDR_A2	SSTL_O	DDR Analog IO	DDR Address
T24	DDR_A3	SSTL_O	DDR Analog IO	DDR Address
AD22	DDR_A4	SSTL_O	DDR Analog IO	DDR Address
U25	DDR_A5	SSTL_O	DDR Analog IO	DDR Address
AC22	DDR_A6	SSTL_O	DDR Analog IO	DDR Address
U24	DDR_A7	SSTL_O	DDR Analog IO	DDR Address
AC23	DDR_A8	SSTL_O	DDR Analog IO	DDR Address
V23	DDR_A9	SSTL_O	DDR Analog IO	DDR Address
AC24	DDR_A10	SSTL_O	DDR Analog IO	DDR Address
AE24	DDR_A11	SSTL_O	DDR Analog IO	DDR Address
AD25	DDR_A12	SSTL_O	DDR Analog IO	DDR Address

W23	DDR_A13	SSTL_O	DDR Analog IO	DDR Address
AE25	DDR_A14	SSTL_O	DDR Analog IO	DDR4: A14 multiplexed as WE_n, low-level active
AD21	DDR_A15	SSTL_O	DDR Analog IO	DDR4: A15 multiplexed as CAS_n, low-level active
Y24	DDR_A16	SSTL_O	DDR Analog IO	A16 is multiplexed to DDR4 as RAS_n, low-level active For DDR3, it is multiplexed as WE#, low-level active
AA23	DDR_A17	SSTL_O	DDR Analog IO	DDR3: A17 multiplexed as CAS, low-level active
P23	DDR_ACT_N	SSTL_O	DDR Analog IO	DDR3: Control output RAS#, low-level active DDR4: Control output ACT_N, active command, low-level active
T25	DDR_BA0	SSTL_O	DDR Analog IO	DDR3/DDR4: Bank address output[1:0]
AE22	DDR_BA1	SSTL_O	DDR Analog IO	
Y25	DDR_BG0	SSTL_O	DDR Analog IO	DDR3：Bank address output[2] DDR4：Bank Group address output[0]
AB24	DDR_CK_N	SSTL_O	DDR Analog IO	DDR3/DDR4 clock output
AB25	DDR_CK_P	SSTL_O	DDR Analog IO	
AE21	DDR_CKE	SSTL_O	DDR Analog IO	DDR3/DDR4 clock enable output, high-level active
T23	DDR_CSN	SSTL_O	DDR Analog IO	DDR3/DDR4 chip select signal output, low-level active
R23	DDR_ODT	SSTL_O	DDR Analog IO	DDR3/DDR4 terminal connection resistance enable signal , high-level active
U23	DDR_RESETN	SSTL_O	DDR Analog IO	DDR3/DDR4 asynchronous reset output, low-level active
Y23	DDR_RZQ	SSTL_O	DDR Analog IO	DDR3/DDR4 termination reference. It needs to be connected to GND through a 240ohm ±1% resistor.
H23	DDR_DM0	SSTL_O	DDR Analog IO	Data DQ[7:0]mask; DDR3: high-level active DDR4: low-level active
K25	DDR_DQS0N	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[7:0], DQS, is responsible for the sampling of DQ[7:0]
K24	DDR_DQS0P	SSTL_O	DDR Analog IO	
N24	DDR_DQ0	SSTL_B	DDR Analog IO	DDR3/DDR4 Data DQ[7:0]
E24	DDR_DQ1	SSTL_B	DDR Analog IO	
P25	DDR_DQ2	SSTL_B	DDR Analog IO	
D25	DDR_DQ3	SSTL_B	DDR Analog IO	
J23	DDR_DQ4	SSTL_B	DDR Analog IO	
D24	DDR_DQ5	SSTL_B	DDR Analog IO	
P24	DDR_DQ6	SSTL_B	DDR Analog IO	
D23	DDR_DQ7	SSTL_B	DDR Analog IO	
N25	DDR_DM1	SSTL_O	DDR Analog IO	Data DQ[15:8]mask; DDR3: high-level active DDR4: low-level active
G25	DDR_DQS1N	SSTL_O	DDR Analog IO	The strobe signal of DDR3/DDR4 data DQ[15:8], DQS1, is responsible for the sampling of DQ[15:8]
G24	DDR_DQS1P	SSTL_O	DDR Analog IO	
H24	DDR_DQ8	SSTL_B	DDR Analog IO	DDR3/DDR4 Data DQ[15:8]
L24	DDR_DQ9	SSTL_B	DDR Analog IO	
E25	DDR_DQ10	SSTL_B	DDR Analog IO	

N23	DDR_DQ11	SSTL_B	DDR Analog IO	
F23	DDR_DQ12	SSTL_B	DDR Analog IO	
M23	DDR_DQ13	SSTL_B	DDR Analog IO	
E23	DDR_DQ14	SSTL_B	DDR Analog IO	
L23	DDR_DQ15	SSTL_B	DDR Analog IO	

Table 2-3 PON Interface Pins

Pin No.	Name	IO Type	Default Value	Description
Y4	XPON_CLKN	AI	Serdes Differential IO	PON SerDes reference clock input, alternative pin, can be left floating
W4	XPON_CLKP	AI	Serdes Differential IO	
AA1	XPON_DINN	AI	Serdes Differential IO	PON SerDes receive signal, AC coupling required, 100ohm ±10% differential impedance
AA2	XPON_DINP	AI	Serdes Differential IO	
W1	XPON_DOUTN	AO	Serdes Differential IO	PON SerDes transmit signal, AC coupling required, 100ohm ±10% differential impedance
W2	XPON_DOUTP	AO	Serdes Differential IO	
U7	XPON_APROBE	AO	Serdes Analog IO	SerDes test pin, can be floated when not in use
T7	XPON_RREF	AO	Serdes Analog IO	PON power reference resistor, need to connect 5.6K±1% to GND
AC3	RX_PWRDOWN	ITOT	PULLDOWN	Optical module receive direction power control signal, output high level voltage to turn on the optical module receive direction power, low level voltage to turn off the receive direction power
AD2	TX_PWRDOWN	ITOT	PULLUP	Optical module transmit direction power control signal, output high level voltage to turn off the optical module receive direction power, low level voltage to turn on the transmit direction power
U3	PON_BEN	ITOT	NA	Optical module Burst enable signal, polarity can be matched
AD1	RX_LOS	ITOT	NA	The optical module receives the detection signal input
AB3	TX_SD	ITOT	NA	The optical module sends detection signal input

Table 2-4 USB Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AE3	USB2_DM	AIO	USB2.0 Analog IO	USB2.0 high-speed sending and receiving signals
AE2	USB2_DP	AIO	USB2.0 Analog IO	
AD3	USB2_RREF	AIO	USB2.0 Analog IO	USB2 power reference resistor, need to connect 4.7K±1% to GND
C4	USB3_DM	AIO	USB3.0 Analog IO	USB3 high-speed sending and receiving signals
B4	USB3_DP	AIO	USB3.0 Analog IO	
D5	USB3_RREF	AIO	USB3.0 Analog IO	USB3 power reference resistor, need to connect 4.7K±1% to GND

A4	USB3_SSRXA	AI	USB3.0 Analog IO	USB3（USB3.x Gen 1）Super high-speed signal reception
A5	USB3_SSRXB	AI	USB3.0 Analog IO	
A1	USB3_SSTXA	AO	USB3.0 Analog IO	USB3（USB3.x Gen 1）Super high-speed signal transmission
A2	USB3_SSTXB	AO	USB3.0 Analog IO	

Table 2-5 PCIe Interface Pins

Pin No.	Name	IO Type	Default Value	Description
AD7	PCIE0_RXM	AI	PCIE2.0 Analog IO	PCIe0 SerDes receive signal, AC coupling is required
AE7	PCIE0_RXP	AI	PCIE2.0 Analog IO	
AC6	PCIE0_TXM	AO	PCIE2.0 Analog IO	PCIe0 SerDes transmit signal, AC coupling is required
AB6	PCIE0_TXP	AO	PCIE2.0 Analog IO	
AB8	LVTX0_CKN	AO	PCIE2.0 Analog IO	PCIe0 100MHz reference clock output
AC8	LVTX0_CKP	AO	PCIE2.0 Analog IO	
AC4	PCIE0_NCLKREQ	ITOT	PULLUP	PCIe0 CLKREQ signal
AB4	PCIE0_RESREF	AIO	PCIE2.0 Analog IO	PCIe0 reference resistor, need to connect 200ohm ±1% to GND
AD4	PCIE0_RSTB	ITOT		PCIe0 reset output
AB10	PCIE1_RXM	AI	PCIE2.0 Analog IO	PCIe1 SerDes receive signal, AC coupling is required
AC10	PCIE1_RXP	AI	PCIE2.0 Analog IO	
AE12	PCIE1_TXM	AO	PCIE2.0 Analog IO	PCIe1 SerDes transmit signal, AC coupling is required
AD12	PCIE1_TXP	AO	PCIE2.0 Analog IO	
AD9	LVTX1_CKN	AO	PCIE2.0 Analog IO	PCIe1 100MHz reference clock output
AE9	LVTX1_CKP	AO	PCIE2.0 Analog IO	
AB12	PCIE1_NCLKREQ	ITOT	PULLUP	PCIe1 CLKREQ signal
AB13	PCIE1_RESREF	AIO	PCIE20 Analog IO	PCIe1 reference resistor, need to connect 200ohm ±1% to GND
AC13	PCIE1_RSTB	ITOT		PCIe1 reset output

Table 2-6 SPIFC Interface Pins

Pin No.	Name	IO Type	Default Value	Description
N1	SPIFC_CLK	ITOT	NA	SPI Flash clock output
R1	SPIFC_CS	ITOT	NA	SPI Flash chip select
R3	SPIFC_DAT0	ITOT	NA	SPI Flash D0/ SPI Flash MOSI
P3	SPIFC_DAT1	ITOT	NA	SPI Flash D1/ SPI Flash MISO
N3	SPIFC_DAT2_WPN	ITOT	NA	SPI Flash D2/ SPI Flash WP
N2	SPIFC_DAT3_HOLD	ITOT	NA	SPI Flash D3/ SPI Flash HOLD

Table 2-7 SPI Interface Pins

Pin No.	Name	IO Type	Default Value	Description
C6	SSP0_FS0	ITOT	NA	SPI select signal, can be used as SPI interface in PCM mode
A8	SSP0_FS1	ITOT	NA	
E3	SSP0_FS2	ITOT	NA	
D2	SSP0_FS3	ITOT	NA	
B7	SSP0_RXD	ITOT	NA	SPI receives data, can be used as SPI interface in PCM mode
C7	SSP0_SCLK	ITOT	NA	SPI clock output, can be used as SPI interface in PCM mode
A7	SSP0_TXD	ITOT	NA	SPI transmit data, can be used as SPI interface in PCM mode

Table 2-8 PCM Interface Pins

Pin No.	Name	IO Type	Default Value	Description
C9	PCM_CLK	ITOT	NA	PCM clock output
B8	PCM_FS	ITOT	NA	PCM sync frame signal, ISI mode can be left floating
C10	PCM_RXD	ITOT	NA	PCM receive signal
B10	PCM_TXD	ITOT	NA	PCM transmit signal

Table 2-9 RGMII Interface Pins

Pin No.	Name	IO Type	Default Value	Description
G1	RGM_TXD3	ITOT	NA	RGMIII interface transmit data
G3	RGM_TXD2	ITOT	NA	RGMIII interface transmit data
H3	RGM_TXD1	ITOT	NA	RGMIII interface transmit data
J3	RGM_TXD0	ITOT	NA	RGMIII interface transmit data
G2	RGM_TXCTL	ITOT	NA	RGMII interface transmit control
K3	RGM_TXCLK_IN	ITOT	NA	MII mode clock input, can be floated when not in use
J1	RGM_TXCLK	ITOT	NA	RGMII interface transmit clock
K2	RGM_RXD3	ITOT	NA	RGMII interface receive data
K1	RGM_RXD2	ITOT	NA	RGMII interface receive data
L3	RGM_RXD1	ITOT	NA	RGMII interface receive data
M3	RGM_RXD0	ITOT	NA	RGMII interface transmit data
M2	RGM_RXCTL	ITOT	NA	RGMII interface receive control
M1	RGM_RXCLK	ITOT	NA	MII mode clock input, can be floated when not in use

Table 2-10 Other Interface Pins

Pin No.	Name	IO Type	Default Value	Description
T2	XTAL_IN	AI	NA	Crystal IO input terminal, external 25MHZ crystal oscillator circuit
T1	XTAL_O	AO	NA	Crystal IO output terminal, external 25MHZ crystal oscillator circuit
C2	X_OSC_I	AI	NA	Reserve
C1	X_OSC_O	AO	NA	Reserve
D3	VDT_VIN	AI	NA	Dying Gasp analog input
AC15	TEST_MODE	IT	PULLDOWN	Test mode configuration, 0: chip works normally, 1: chip test mode
AD19	UART0_RX	ITOT	NA	Dying Gasp analog input
AE19	UART0_TX	ITOT	NA	Test mode configuration, 0: chip works normally, 1: chip test mode
AE15	UART1_RX	ITOT	NA	UART0 receive signal pin
AD15	UART1_TX	ITOT	NA	UART0 transmit signal pin
V3	I2C0_SCL	ITOT	PULLUP	UART1 receive signal pin
V2	I2C0_SDA	ITOT	PULLUP	UART1 transmit signal pin
AD16	I2C1_SCL	ITOT	PULLUP	I2C0 clock output signal, need external pull-up resistor
AE16	I2C1_SDA	ITOT	PULLUP	I2C0 data transmission and reception signal, need external pull-up resistor
AD18	X_P0_LED0	ITOT	NA	GEPHY Port0 LED0, function register configurable
D21	X_P0_LED1	ITOT	NA	GEPHY Port0 LED1, function register configurable
AE18	X_P1_LED0	ITOT	NA	GEPHY Port1 LED0, function register configurable
D18	X_P1_LED1	ITOT	NA	GEPHY Port1 LED1, function register configurable
AC19	X_P2_LED0	ITOT	NA	GEPHY Port2 LED0, function register configurable
AC20	X_P3_LED0	ITOT	NA	GEPHY Port3 LED0, function register configurable
AC14	RSTN	ITOT	PULLUP	Chip hardware reset input, requires an external reset circuit or pull-up resistor.
F3	RST_OUT	ITOT	PULLUP	Chip reset output
M4	GPIO_7	ITOT	NA	Normal GPIO
AC18	USB3_PWR_OC	ITOT	NA	USB3.0 power over-current detection input
F1	CLK8K_OUT/ MDC1	ITOT	NA	8KHZ clock output/MDIO data cable
F2	PTP_1PPS/ MDIO1	ITOT	NA	1PPS output/MDIO data cable
AB21	USB2_VBUS	ITOT	NA	USB2.0 VBUS detection input
AB20	USB2_DRVBUS	ITOT	NA	USB2.0 VBUS power supply control enable
AB15	USB3_VBUS	ITOT	NA	USB3.0 VBUS detection input
T4	USB3_PWR_EN	ITOT	NA	USB3.0 VBUS power supply control enable
AB16	DYINGOUT	ITOT	PULLUP	Power-Off alarm output

AB14	UART2_RXD	ITOT	PULLUP	UART2 data receiver
AC17	UART2_TXD	ITOT	POLLDOWN	UART2 data transmitter
AB18	UART2_CTS	ITOT	NA	UART2 hard flow control
AC16	UART2_RTS	ITOT	PULLUP	UART2 hard flow control
AB16	DYINGOUT	ITOT	PULLUP	Power off alarm output
H4	VQPS_EFUSE	AIO	NA	Test pin, floating

Table 2-11 Power Ground

Pin No.	Quantity	Name	IO Type	Description
G8,G9,G10,H9,H10,H11,H12,J7,K7,L7	10	VCC3IO	PG	3.3V IO power(10 pins)
G11,G14,G15	3	VCC33A_GPHY	PG	GPHY 3.3V analog power(3 pins)
W7	1	USB2VCC33A	PG	USB2 3.3V analog power
G7	1	USB3VCC33A	PG	USB3 3.3V analog power
N7,N8,W13,W14	4	VCC18	PG	1.8V power(4 pins)
V7	1	VCC18A_PON	PG	PON 1.8V analog power
W8	1	USB2VCC18A	PG	USB2 1.8V analog power
H8	1	USB3VCC18A	PG	USB3 1.8V analog power
W9	1	TDC_VCC18A	PG	Temperature sensor 1.8V analog power
R7	1	PLL_VCC18A	PG	PLL 1.8V analog power
M7	1	XTAL_VCC18	PG	Crystal 1.8V analog power
H7	1	VDT_VCC18A	PG	VDT 1.8V power
W11	1	PCIE0_VPH	PG	PCIe 1.8V power
W12	1	PCIE1_VPH	PG	
K18,K19	2	LDO_VCC18A	PG	Internal LDO input
L18,L19	2	LDO_O_VCC12A	PG	Internal LDO output, voltage 1.2V-1.5V.
M19,N19,P19,R19,U19,V19,W19	7	VDDQ	PG	DDR3/DDR4 IO voltage: DDR3: connect to 1.5V DDR4: connect to 1.2V (7 pins)
G12,G13,H13,H14,H15,H16,H17,H18,H19	9	VCCK11	PG	GPHY 1.1V supply voltage (9 pins)
G16,G17,G18	3	VCC11A_GPHY	PG	GPHY 1.1V analog voltage (3 pins)
L8,M8,M18,N18,P7,P8,P18,R18,T8, V14,V15,V16,V17,W15,W16,W17	16	VCCK	PG	0.9V supply voltage(16pins)
V12	1	VCC_VP0	PG	0.9V PCIe0 supply voltage

V13	1	VCC_VP1	PG	0.9V PCIe1 supply voltage
V8,U8	2	VCC09A_PON	PG	0.9V PON analog voltage
K8	1	USB3VCC09A_RX	PG	0.9V USB3 receive supply voltage
J8	1	USB3VCC09A_TX	PG	0.9V USB3 transmit supply voltage
R8	1	PLL_VCC	PG	0.9V PLL supply voltage
V11	1	LVTX_VCC09A	PG	0.9V PCIe reference clock supply voltage
T19	1	DDR_PLLVCCA	PG	1.8V DDR PLL voltage
A10 B1,B2,B5 C3,C5,C8,C17,C22,C23 D1,D4,D6,D7,D8,D9,D10,D11,D12,D13,D14,D16,D17,D19,D20,D22 E4,E22 F4,F22 G4,G22,G23 H22,H25 J2,J4,J18,J19,J22 K4,K10,K11,K12,K13,K14,K15,K16,K22,K23 L4,L10,L12,L14,L16,L22,L25 M10,M11,M12,M13,M14,M15,M16,M22 N4,N10,N12,N14,N16,N22 P4,P10,P11,P12,P13,P14,P15,P16,P22 R2,R12,R14,R16,R22 T3,T10,T11,T12,T13,T14,T15,T16,T18,T22 U4,U18,U22 V4,V9,V18,V22 W18,W22 Y22 AA4,AA22 AB5,AB7,AB9,AB11,AB17,AB19,AB22,AB23 AC5,AC7,AC9,AC11,AC12,AC21,AC25 AD6,AD10,AD13 AE1,AE4,AE6,AE10,AE13	130	VSS	PG	Power ground
V1,Y1,Y2,AB2,AB1,W3,AA3,Y3	8	GNDA_PON	PG	PON Serdes analog power ground
R4,R10	2	PLL_GND	PG	PLL power ground
W10	1	LVTX_GND09A	PG	PCIe reference clock analog ground
V10	1	TDC_GNDA	PG	Temperature sensor ground

Notes:

The pull-up and pull-down resistor values：

PULLUP: 40-kΩ

PULLDOWN: 40-kΩ

NA: By default, there is no pull-up and drop-down settings

2.3 Pin Sharing Schemes

Table 2-12 GPIO Multiplexed Pin Options

Pin No.	Name	Default Function		2nd Function		3rd Function	
		Name	Direction	Name	Direction	Name	Direction
F3	RST_OUT	RST_OUT	OUT			GPIO_0	INOUT
AB14	UART2_RXD		IN	UART2_RXD	IN	GPIO_1	INOUT
AC17	UART2_TXD		OUT	UART2_TXD	OUT	GPIO_2	INOUT
AB18	UART2_CTS		IN	UART2_CTS	IN	GPIO_3	INOUT
AC16	UART2_RTS		IN	UART2_RTS	OUT	GPIO_4	INOUT
AB16	DYINGOUT		IN	DYINGOUT	OUT	GPIO_5	INOUT
C6	SSP0_FS0	SSP0_FS0	OUT	STRAP_BOOT_MODE1	IN	GPIO_9	INOUT
A8	SSP0_FS1	SSP0_FS1	OUT	STRAP_XIP_SEL	IN	GPIO_10	INOUT
E3	SSP0_FS2	SSP0_FS2	OUT	STRAP_NAND_ECC	IN	GPIO_11	INOUT
D2	SSP0_FS3	SSP0_FS3	OUT	STRAP_NAND_ADDR_CYC	IN	GPIO_12	INOUT
B7	SSP0_RXD	SSP0_RXD	IN	STRAP_NAND_PAGE_SIZE	IN	GPIO_13	INOUT
A7	SSP0_TXD	SSP0_TXD	OUT	STRAP_BOOT_MODE0	IN	GPIO_14	INOUT
C7	SSP0_SCLK	SSP0_SCLK	OUT			GPIO_15	INOUT
C9	PCM_CLK	PCM_CLK	OUT	PSCLK	OUT	GPIO_16	INOUT
B8	PCM_FS	PCM_FS	OUT			GPIO_17	INOUT
B10	PCM_TXD	PCM_TXD	OUT	ISI_MOSI	OUT	GPIO_18	INOUT
C10	PCM_RXD	PCM_RXD	IN	ISI_MISO	IN	GPIO_19	INOUT
R1	SPIFC_CS	SPIFC_CS	OUT	NAND_Ren	OUT	GPIO_20	INOUT
N1	SPIFC_CLK	SPIFC_CLK	OUT	NAND_CEn	OUT	GPIO_21	INOUT
R3	SPIFC_DAT0	SPIFC_DAT0	INOUT	NAND_CLE	OUT	GPIO_22	INOUT
P3	SPIFC_DAT1	SPIFC_DAT1	INOUT	NAND_WEn	OUT	GPIO_23	INOUT
N3	SPIFC_DAT2_WPN	SPIFC_DAT2_WPN	INOUT	NAND_ALE	OUT	GPIO_24	INOUT

N2	SPIFC_DAT3_HOLD	SPIFC_DAT3_HOLD	INOUT	NAND_RDY_BUSY	IN	GPIO_25	INOUT
AD19	UART0_RX	UART0_RX	IN	RGM_RXER	IN	GPIO_26	INOUT
AE19	UART0_TX	UART0_TX	OUT	RGM_TXER	OUT	GPIO_27	INOUT
AE15	UART1_RX	UART1_RX	IN	PON_BEN_INV	OUT	GPIO_28	INOUT
AD15	UART1_TX	UART1_TX	OUT	RGM_CRS	IN	GPIO_20	INOUT
V3	I2C0_SCL	I2C0_SCL	INOUT			GPIO_30	INOUT
V2	I2C0_SDA	I2C0_SDA	INOUT			GPIO_31	INOUT
AD16	I2C1_SCL	I2C1_SCL	INOUT	debug_sysclk[0]	OUT	GPIO_32	INOUT
AE16	I2C1_SDA	I2C1_SDA	INOUT	debug_sysclk[1]	OUT	GPIO_33	INOUT
K3	RGM_TXCLK_IN	RGM_TXCLK_IN	OUT	DYINGIN	IN	GPIO_6	INOUT
J1	RGM_TXCLK	RGM_TXCLK	OUT	NAND_ADQ0	INOUT	GPIO_34	INOUT
G2	RGM_TXCTL	RGM_TXCTL	OUT	NAND_ADQ1	INOUT	GPIO_35	INOUT
J3	RGM_TXD0	RGM_TXD0	OUT	NAND_ADQ2	INOUT	GPIO_36	INOUT
H3	RGM_TXD1	RGM_TXD1	OUT	NAND_ADQ3	INOUT	GPIO_37	INOUT
G3	RGM_TXD2	RGM_TXD2	OUT	NAND_ADQ4	INOUT	GPIO_38	INOUT
G1	RGM_TXD3	RGM_TXD3	OUT	NAND_ADQ5	INOUT	GPIO_39	INOUT
M3	RGM_RXD0	RGM_RXD0	IN	NAND_ADQ6	INOUT	GPIO_40	INOUT
L3	RGM_RXD1	RGM_RXD1	IN	NAND_ADQ7	INOUT	GPIO_41	INOUT
K1	RGM_RXD2	RGM_RXD2	IN			GPIO_42	INOUT
K2	RGM_RXD3	RGM_RXD3	IN			GPIO_43	INOUT
M2	RGM_RXCTL	RGM_RXCTL	IN			GPIO_44	INOUT
M1	RGM_RXCLK	RGM_RXCLK	IN			GPIO_45	INOUT
AB3	TX_SD	TX_SD	OUT			GPIO_46	INOUT
AD1	RX_LOS	RX_LOS	IN			GPIO_47	INOUT
U3	PON_BEN	PON_BEN	OUT			GPIO_48	INOUT
AD2	TX_PWRDOWN	TX_PWRDOWN	OUT			GPIO_49	INOUT
AC3	RX_PWRDOWN	RX_PWRDOWN	OUT			GPIO_50	INOUT
AD4	PCIE0_RSTB	PCIE0_RSTB	OUT			GPIO_51	INOUT
AC4	PCIE0_nCLKREQ	PCIE0_nCLKREQ	INOUT			GPIO_52	INOUT
AC13	PCIE1_RSTB	PCIE1_RSTB	OUT			GPIO_53	INOUT
AB12	PCIE1_nCLKREQ	PCIE1_nCLKREQ	INOUT			GPIO_54	INOUT
M4	GPIO7	GPIO7	INOUT	RGM_COL	IN	GPIO_7	INOUT
AC18	USB3_PWR_OC	USB3_PWR_OC	IN			GPIO_8	INOUT
F1	CLK8K_OUT	CLK8K_OUT	OUT	MDC1	OUT	GPIO_57	INOUT
F2	PTP_1PPS	PTP_1PPS	OUT	MDIO1	INOUT	GPIO_58	INOUT
AB21	USB2_VBUS	USB2_VBUS	IN			GPIO_59	INOUT
AB20	USB2_DRVBUS	USB2_DRVBUS	OUT			GPIO_60	INOUT
AB15	USB3_VBUS	USB3_VBUS	IN			GPIO_61	INOUT
T4	USB3_PWR_EN	USB3_PWR_EN	OUT			GPIO_62	INOUT

3 BOOT Mode

Support four Boot modes as followed:

Table 3-1 Boot mode

Name	Selection			
STRAP_BOOT_MODE0	0	0	1	1
STRAP_BOOT_MODE1	0	1	0	1
Boot Mode	UART0 boot	SPI NAND boot	Parallel NAND boot	SPI NOR boot

Table 3-2 Boot parameter

STRAP_NAND_PAGE_SIZE	0:2K bytes 1:4K bytes
STRAP_NAND_ADDR_CYC	Parallel NAND/SPI NAND 0:2-cycle/3-byte mode 1:3-cycle/4-byte mode
STRAP_XIP_SEL	0: dummy after the address 1: dummy in front of the address Parallel NAND: 0: Disable ECC 1: Enable ECC, ECC configuration follow STRAP_NAND_ECC configuration
STRAP_NAND_ECC	NAND 0:ECC 4-bit 1:ECC 8-bit

4 Features Description

4.1 SOC Subsystem

4.1.1 Processor

The chip has a multi-core high-performance processor and a maximum operating frequency of 1Ghz, which can meet various PON business applications.

4.1.2 DDR3/4

The system integrates a DDR3/DDR4 combo controller and PHY, supporting the following features:

☐ Supports 16-bit IO width

☐ Supports DDR3/4-1600

4.1.3 PCIE2.0

The chip supports 2 PCIE2.0 interfaces with a maximum rate of 5Gbps and can be plugged into a WIFI chip for WIFI access.

4.1.4 USB3.0

The chip integrates a USB3.0 controller and supports the following features:

☐ USB3.0 host mode

☐ Supports USB3.0 device, device mode is option

☐ Supports USB2.0 and USB1.1 devices through hub extension

☐ Supports low power consumption mode

4.1.5 USB2.0

The chip integrates a USB2.0 controller and supports the following features:

☐ USB2.0 host mode
☐ Supports USB2.0 device, device mode is option
☐ Compatible with USB1.1 devices
☐ Supports low power consumption mode

4.1.6 NAND

The chip supports parallel port NAND devices:
☐ Supports standard compatible ONFI NAND devices, including ONFI3 and below
☐ Supports maximum capacity 4GB
☐ Block size supports 8K~2048KB
☐ Page sizes supports 512B~8KB, but do not supports 512B when booting
☐ ECC and page size settings can be configured via strap
☐ Maximum support ECC error correction to 8bit

4.1.7 SPIFC

The chip integrates SPI flash controller to realize external Norflash or Nandflash device.
☐ Supports AXI/AHB interface
☐ Supports DTR mode
☐ Supports DMA handshake mode and CPU PIO mode
☐ Supports DUAL/QUAD output mode, also supports DUAL/QUAD IO mode
☐ Only supports Single-IO mode
☐ Support SPI working frequency programmable setting
☐ Support SPI NOR/NAND command port command mode

4.1.8 GPIO

Programmable general purpose IO controllers that can be programmed for each GPIO pin to meet differentiated requirements.
☐ Support for up to 63 GPIOs programmable
☐ 32 GPIOs can all trigger GPIO interrupts independently
☐ Interrupts of the GPIOs that support interrupts all support edge-triggered, level-triggered
☐ Each GPIO can supports configuration to high or low level
☐Each GPIO output data is independently set or cleared
☐ All GPIO ports can be set as inputs after a hardware reset

When GPIO supports interrupts, the de-bounce function can be configured.

4.1.9 I2C

The I2C module supports CPU configuration in master mode or slave mode.
☐ Supports I2C standard mode, fast mode and fast + mode
☐ Supports HS high-speed mode
☐ Supports 7/10bit address searching
☐ Supports Glitch-Free
☐ Supports programmable slave address
☐ Support master-TX, master-RX, slave-TX and slave-RX modes

4.1.10 UART

UART is an asynchronous serial communication control module and supports infrared control mode.. It is compatible with 16550 protocol.
☐ Compatible with high-speed NS 16C550A protocol
☐ Supports infrared 1.3 SIR, the rate can reach 115kbps
☐ Supports programmable SIR pulse width of 1.6us or 3/16 baud rate pulse width
☐ Supports multi-frame transmission mechanism in FIR mode
☐ The hardware configurable FIFO depth is fixed at 128
☐ Supports internal diagnostic mechanisms
☐ Supports interrupt, polarity, overflow and frame error emulation
☐ Supports CRC error and physical error simulation in FIR mode
☐ Supports flow control RTS/CTS, but need to reserve the pin RTS/CTS

4.1.11 WDT

In the conventional WDT design, in order to prevent the CPU software from entering a deadlock, when the software cannot input WatchDog Timer regularly, the system can be reset so that it can be restarted.
☐ After timing out, the following signals can be output
1）System reset;
2）System interruption;
3）External interrupt;

☐ 32-bit down counter
☐ Internal or external clock source can be selected
☐ Output reset width period is configurable
☐ Access protection registers are set

4.1.12 TIMER

The timer module provides 4 sub-timer settings, which are independent of each other. Timing can be incremented or decremented with PCLK or EXTCLK. Whether to issue a timer interrupt depends on the register settings.
☐ Four 32-bit timing configurations
☐ Optional 32.768KHz or 25Mhz working clock
☐ Issue an interrupt after overflow and the timer is reached
☐ Each sub-timer has 2 match register settings
☐ Support timed increment or decrement

4.1.13 MDIO

Used to control the external GEPHY two-wire interface.

4.1.14 TDM/SPI/ISI

Voice interface, two working modes:
TDM+SPI mode: use 4 lines of TDM and SPI to connect with SLIC chip to realize voice communication
ISI mode: use ISI interface 3 lines to connect with SLIC chip to realize voice communication.

4.2 ONU Subsystem

SOC chip implementing Layer2 switching and Layer3/4 hardware NAT/NAPT functionality with four Gigabit Ethernet interfaces and DDR3/DDR4 particle support for low cost home gateway functionality. The chip supports Layer2 and supports Layer3 NAT/NAPT hardwired network switching. The chip can be used for various service application functions on the upper layer of the processor such as DHCP, HTTP and some services that require the use of hardwired forwarding functions.

The chip has built-in powerful protocol analysis functions and can handle various hard forwarding services such as VLAN, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP and IGMP messages. For VLAN and PPPoE protocols, the chip supports automatic encapsulation and decapsulation of VLAN tagged frames and

PPPoE headers.

The chip supports port-based, protocol-based, VLAN-based, etc. It supports up to 4,000 VLAN groups and supports the SPAN tree protocol, whose states can be divided into four: forbidden, blocking, listening and forwarding.

5 Interface Timing and Characteristics

5.1 SPI Interface Timing

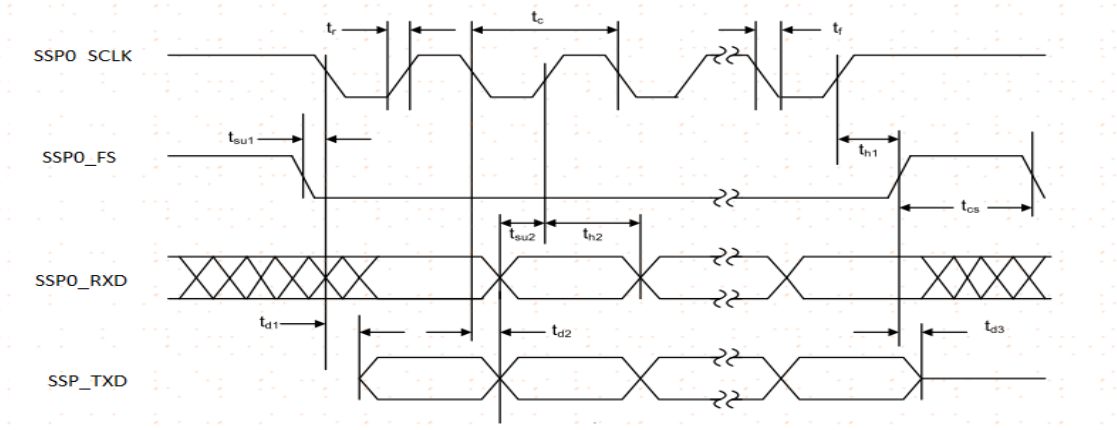


Figure 5-1 SPI Interface Timing

Table 5-1

Symbol	Parameter	Min.	Typ.	Max.	Units
Tc	Cycle time SSP0_SCLK	62	--	--	ns
Tr	Rise time of SSP0_SCLK	--	--	25	ns
Tf	Fall time of SSP0_SCLK	--	--	25	ns
Td1	Delay time,SSP0_SCLK fall to SSP0_TXD active	--	--	20	ns
Td2	Delay time,SSP0_SCLK fall to SSP0_TXD transition	--	--	20	ns
Td3	Delay time,SSP0_FS rise to SSP0_TXD tristate	--	--	20	ns
Tsu1	Setup time,SSP0_FS to SSP0_SCLK fall	25	--	--	ns
Th1	Hold time,SSP0_FS to SSP0_SCLK rise	20	--	--	ns
Tsu2	Setup time,SSP0_RXD to SSP0_SCLK rise	25	--	--	ns
Th2	Hold time,SSP0_RXD to SSP0_SCLK rise	20	--	--	ns
Tcs	Delay time between chip selects	220	--	--	ns

5.2 MDIO Interface Timing

Receive:

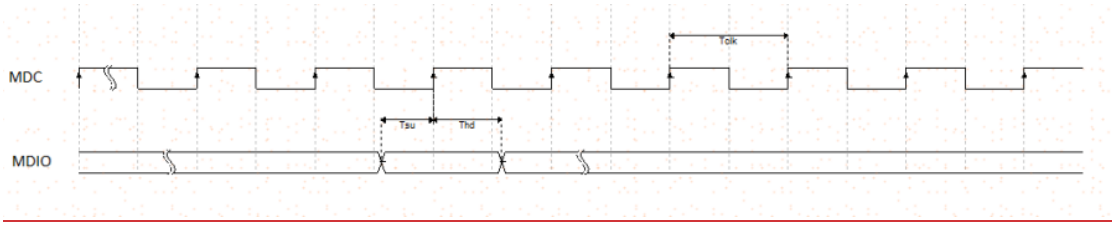


Figure 5-2 MDIO Interface Receive Timing

Transmit:

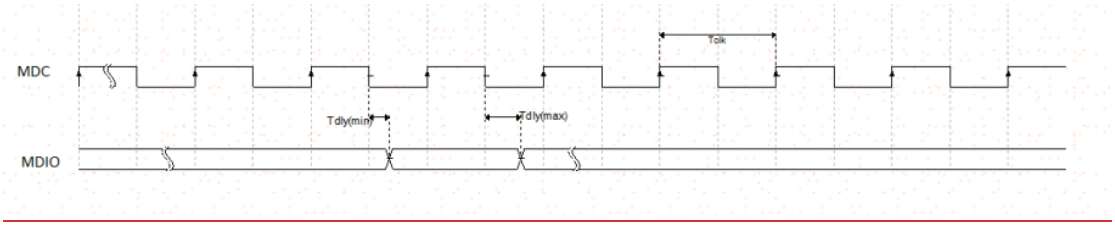


Figure 5-3 MDIO Interface Transmit Timing

Table 5-2

Symbol	Parameter	Min.	Typ.	Max.	Units
Tclk	MDC clock cycle	2500	2000	-	ns
Tsu	Setup time for input	10	-	-	ns
Thd	Hold time for input	10	-	-	ns
Tdly	Delay time for output	--		1000	ns

5.3 I2C Interface Timing

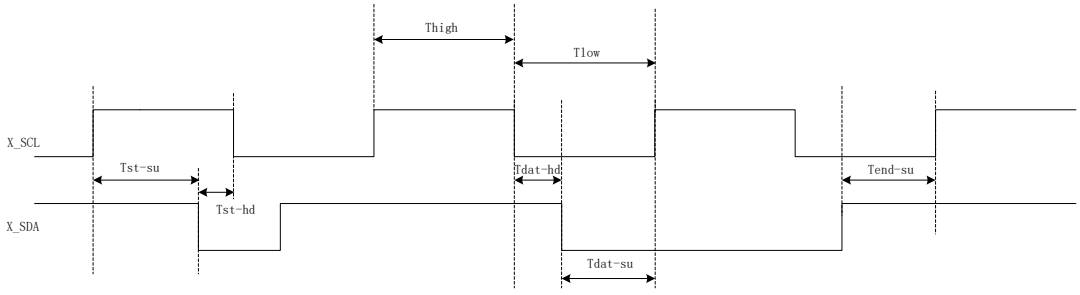


Figure 5-4 I2C Interface Timing

Table 5-3

Symbol	Name	Standard mode		Fast mode		Units
		Min.	Max.	Min.	Max.	
fscl	Clock frequency		100		400	Khz
Tlow	Clock low-level voltage time	4.7		1.3		us
Thigh	Clock high-level voltage time	4.0		0.6		us
Tst-su	Setup time for start	4.7		0.6		us
Tst-hd	hold time for start	4.0		0.6		us
Tdat-su	Setup time for data	250		100		ns
Tdat-hd	Hold time for data	5.0	3.45	0	0.9	us
Tend-su	Setup time for end	4.0		0.6		us

Note：Tdat-hd uses the Max value(3.45us) only when the SCL Tlow is not extended.

5.4 TDM/PCM Interface Timing

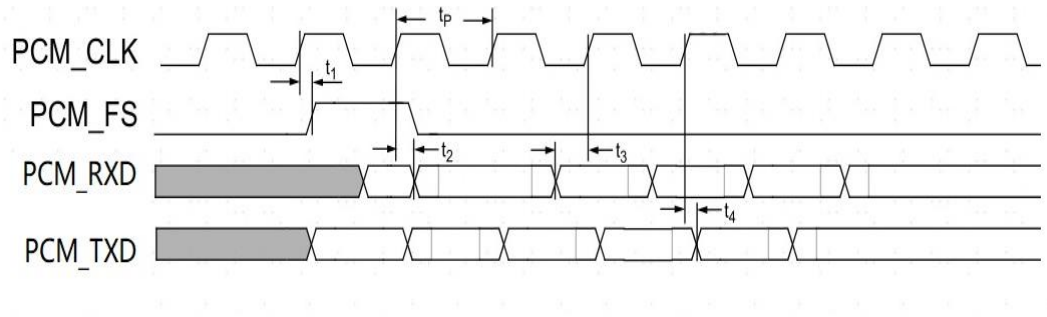


Figure 5-5TDM/PCM Interface Timing

Table 5-4

Symbol	Parameter	Min.	Typ.	Max.	Units
t_p	PCLK Period	--	2.048 /4.096	--	Mhz
t1	Delay time:PCM_CLK rising edge to PCM_FS asserted	-20	--	25	ns
t2	Hold time:PCM_CLK sample edge to PCM_RXD transition	0	--	--	ns
t3	Setup time:PCM_RXD valid to PCM_CLK sample edge	20	--	--	ns
t4	Delay time:PCM_CLK rising edge to PCM_TXD asserted	-20	--	25	ns

Note: PCM_CLK allows the inversion, if the SOC chip sends data with the falling edge, the peer must use the rising edge to sample the data, and vice versa.

5.5 ISI Interface Timing

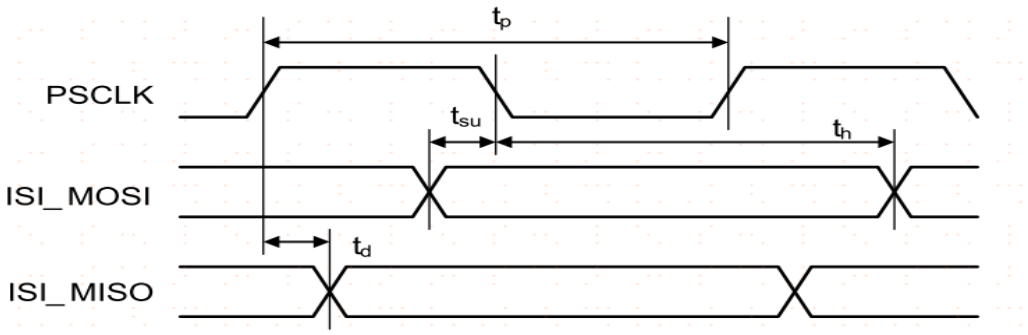


Figure 5-6 ISI Interface Timing

Table 5-5

Symbol	Parameter	Min.	Typ.	Max.	Units
tsu	Setup Time, ISI_MOSI to PSCLK Fall	7.5	--	--	ns
th	Hold Time, ISI_MOSI to PSCLK Fall	5	--	--	ns
td	Delay Time, PSCLK Rise to ISI_MISO	--		16	ns
tp	PSCLK Period	--	40.69	--	ns

5.6 SPI FLASH Interface Timing

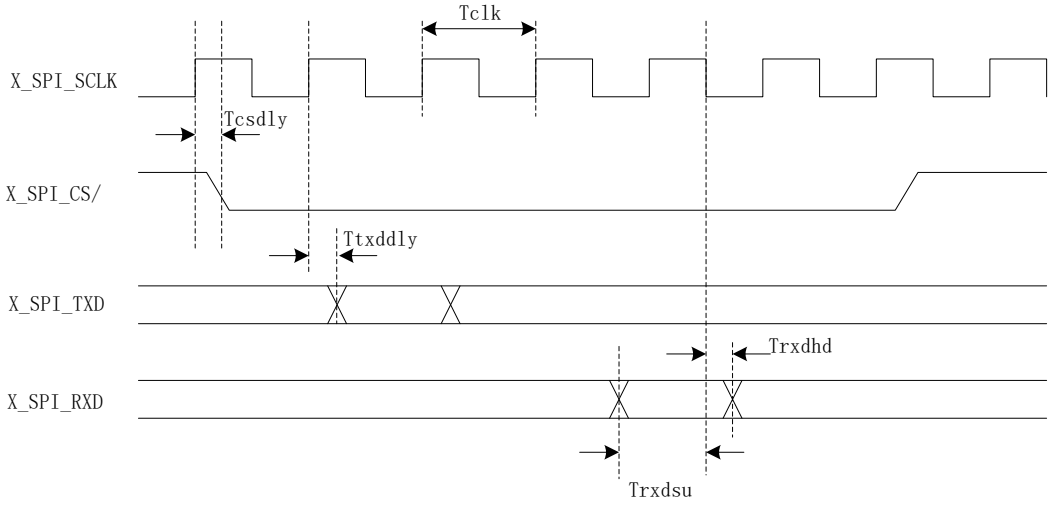


Figure 5-7 SPIFC Interface Timing

Table 5-6

Description	Symbol	Min.	Typ.	Max.	Units
X_SPI_SCLK clock cycle	Tclk	20	40	-	ns
Setup time for input	Trxdsu	10	-	-	ns
Hold time for input	Trxdhd	2	-	10	ns
Delay time for output @50Mhz,15pF	Ttxddly Tcsdly	-	-	8	ns

Note: The receiving direction uses the falling edge to sample the data.

5.7 NAND Interface Timing

Table 5-7 NAND AC Timing Characteristics for Command / Address / Data Input

Symbol	Parameter	Min.	Typ.	Max.	Units
tCLS	CLE setup time	12	-	-	ns
tCLH	CLE hold time	5	-	-	ns
tCS	-CE Setup time	20	-	-	ns
tCH	-CE hold time	5	-	-	ns
tWP	-WE pulse width	12	-	-	ns
tALS	ALE setup time	12	-	-	ns
tALH	ALE hold time	5	-	-	ns
tDS	Data setup time	12	-	-	ns
tDH	Data hold time	5	-	-	ns
tWC	Write cycle time	25	-	-	ns
tWH	-WE high hold time	10	-	-	ns
tADL	Addess to data loading time	100	-	-	ns

Table 5-8 AC Characteristics for Operation

Symbol	Parameter	Min.	Typ.	Max.	Units
tR	Data transfer from cell to register	-	-	25	us
tAR	ALE to -RE delay	10	-	-	ns
tCLR	CLE to -RE delay	10	-	-	ns
tRR	Ready to -RE low	20	-	-	ns
tRP	-RE pulse width	12	-	-	ns
tWB	-WE high to busy	-	-	100	ns
tWW	-WP low to -WE low	100	-	-	ns
tRC	Read cycle time	25	-	-	ns
tREA	-RE access time	-	-	20	ns
tCEA	-CE access time	-	-	25	ns
tRHZ	-RE high to output Hi-Z	-	-	100	ns

tCHZ	-CE high to output Hi-Z	-	-	30	ns
tCSD	-CE high to ALE or CLE don't care	0	-	-	ns
tRHOH	-RE high to output hold	15	-	-	ns
tRLOH	-RE low to output hold	5	-	-	ns
tCOH	-CE high to output hold	15	-	-	ns
tREH	-RE high hold time	10	-	-	ns
tIR	Output hi-Z to -RE low	0	-	-	ns
tRHW	-RE high to -WE low	100	-	-	ns
tWHR	-WE high to -RE low	60	-	-	ns

5.8 USB2.0 Interface Characteristics

Table 5-9 USB2.0 Transmit DC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
High-speed Input Level						
Vhsdiff	High-speed deifferential input sensitivity	|Vi(dp) - Vi(dm)| Measured at the connecttion as an appplication circuit	300	-	-	mV
Vhscm	High-speed data signaling common-mode voltage range	-	-50	-	500	mV
Vhssq	High-speed squelch detechtion threshold	-	525	-	625	mV
High-speed Output Level						
Vhsoi	High-speed idle-level output voltage (differential)	-	-20	-	20	mV
Vhsol	High-speed low-level output voltage(differential)	-	-20	-	20	mV
Vhsoh	High-speed low-level output voltage(differential)	-	360	400	440	mV

Vchirpj	Chirp-J output voltage(differential voltage)	-	700	-	1100	mV
Vchirpk	Chirp-K output voltage(differential voltage)	-	-900	-	-500	mV
Idp/dm	Allowable output current of DP/DM lines	When the termination if 45 Ω ± 10%	14.55	17.78	21.79	mA
High-speed Terminating Resistor						
Zhsdrv	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Zhsterm	Differential impedance	-	76.5	90	103.5	Ω

Table 5-10 USB2.0 AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
High-speed Drive Characteristics						
Thsdrat	High-speed TX data rate	-	479.76	-	480.24	Mbps
Thsdrat	High-speed RX data rate	-	479.76	-	480.24	Mbps
tHSR	High-speed differential rise time	10%~90%	100	-	-	ps
tHSF	High-speed differential fall time	10%~90%	100	-	-	ps
High-speed Drive Timing						
	Driver waveform requirement	Please refer to the eye pattern of template 1	Please follow template1 in the USB2.0 specification			
High-speed Receive Timing						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4	Please follow template4 in the USB2.0 specification			

Table 5-11 USB1.1 Transceiver DC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Input level for low-/full-speed						
Vih	High-level input voltage	driven	2.0	-	-	V
Vihz	High-level input voltage	floating	2.7	-	3.6	V
Vil	Low-level input voltage	-	-	-	0.8	V
Vdi	Differential input sensitivity	|Vi(dp) - Vi(dm)	0.2	-	-	V
Vcm	Differential common-mode voltage	Include Vdi range	0.8	-	2.5	V
Input levels for single-ended receiver						
Vse1	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels for low-/full-speed						
Vol	Low-level output voltage	-	0	-	0.3	V
Voh	High-level output voltage	-	2.8	-	3.6	V

Table 5-12 USB1.1 Transceiver AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Driver char for full-speed						
Tfdraths	Full-speed TX data rate	-	11.994	-	12.006	Mbps
Tfdraths	Full-speed RX data rate	-	11.994	-	12.006	Mbps
Driver char for low-speed						
Tldraths	low-speed TX data rate	-	1.49925	-	1.50075	Mbps
Tldraths	low-speed RX data rate	-	1.49925	-	1.50075	Mbps
Driving timing for full-speed						
	Propagation delay(VI,FSE0 OE to DP,DM)	-	-	-	15	ns
Tfdeop	Source jitter from differential	-	-2.0	-	5.0	ns

	transitions to SE0 transition					
Tjr1	Receiver jitter	To the next transition	-18.5	-	18.5	ns
Tjr2	Receiver jitter	For the paired transition	-9.0	-	9.0	ns
Tfeopt	Source SE0 interval of EOP	-	160	-	175	ns
Tfeopr	receiver SE0 interval of EOP	-	82	-	-	ns
Tfst	Width of the SE0 interval during differential transition	-	-	-	14	ns
Driving timing for low-speed						
Tldeop	Source jitter from differential transition to SE0 transition	-	-40	-	100	ns
Tjr1	Receiver jitter	To next transition	-75	-	75	ns
Tjr2	Receiver jitter	For the paired transition	-45	-	45	ns
Tleopt	Source SE0 interval of EOP	-	1.25	-	1.5	us

5.9 USB3.0 Interface Characteristics

Table 5-13 USB3.0 Transmitter Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
UI	Unit interval	-	199.94	200	200.06	ps
Vtx-diff-pp	Differential peak-to-peak TX voltage	2* |Vtxp - Vtxn|,measured at the TX near end	800	-	1200	mV
Vtx-diff-low	Low-power Differential peak-to-peak TX voltage	2* |Vtxp - Vtxn|,measured at the TX near end	400	-	1200	mV
Vtx-de-ratio	TX	-	3.0	-	4.0	dB

	de-emphasis level					
Rtx-diff-dc	DC differentail impedance	-	75	-	200	Ω
Cac-coupling	AC Coupling capacitor	-	75	-	200	nF
Ttx-dj-far	Far-end TX deterministic jitter	Deterministic jtter assuming only the dual-dirac distribution	-	-	0.43	UI
Ttx-rj-far	Far-end TX random jitter	Measured at the TP1 and after receiver quualization function by using the CP1 pattern at 10^{-12} BER	-	-	0.23	UI
Ttx-tj-far	Far-end TX total jitter	Measured at the TP1 and after receiver equalization (Tj=Dj+Rj)	-	-	0.66	UI
Vtdr	The voltage change allowed during the reveiver detection	Total amount of the voltage change during TX-detect-RX	-	-	600	mV

Table 5-14 USB3.0 SSC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Tssc-mod-rate	Modulation rate	-	30	-	33	kHz
Tssc-freq-deviation	SSC deviation	-	+0/-4000	-	+0/-5000	ppm
Tssc-slew-rate	SSC slew rate	-	-	-	10	ms/s

Table 5-15 USB3.0 LFPS Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Tperiod	Period of the LFPS signal	-	20	-	100	ns
Vcm-ac-lfps	Ac common-mode voltage of the LFPS	-	-	-	100	mV
Vtx-diff-pp-lfps	Differential peak-to-peak LFPS voltage swing	2*|Vtxp-Vtxn|	800	-	1200	mV
Vtx-diff-pp-lfps-lp	Low-power differential peak-to-peak LFPS	2*|Vtxp-Vtxn|	400	-	600	mV

Trise-fall-2080	Rise/fall time of the LFPS signal	-	-	-	4.0	ns
Duty cycle	Duty cycle of the LFPS SIGNAL	-	40	-	60	%

Table 5-16 USB3.0 Receiver Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
UI	Unit interval	-	199.94	200	200.06	ps
Rrx-dc	Receiver common-mode impedance	-	18	-	30	Ω
Rrx-diff-dc	Receiver DC differential impedance	-	72	-	120	Ω
Vrx-lfpsdet-diff-pp	LFPS detect threshold	-	100-		300	mV

Table 5-17 USB3.0 RX Input Jitter Tolerance

Symbol	Description	Condition	Min.	Typ.	Max.	Units
F1	Tolerance corner	-	-	4.9	-	MHz
Jrj	Random jitter	-	-	0.0121	-	UI rms
Jrj_p-p	Random jitter peak-to-peak at 10^{-12}	-	-	0.17	-	UIp-p
Jpj_500khz	Sinusoidal jitter	-	-	2.0	-	UIp-p
Jpj_1mhz	Sinusoidal jitter	-	-	1.0	-	UIp-p
Jpj_2mhz	Sinusoidal jitter	-	-	0.5	-	UIp-p
Jpj_f1	Sinusoidal jitter	-	-	0.2	-	UIp-p
Jpj_50mhz	Sinusoidal jitter	-	-	0.2	-	UIp-p

5.10 DDR Interface Characteristics

Table 5-18 DDR Interface Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
Voh	DC output high	-	0.80* VDDQ for DDR3	-	-	V
Vol	DC output low	-	-	-	0.20 * VDDQ for DDR3	V
ODT	120,60,40 ohms	-	-10	typ	+10	-
Ron	34.0/40.0/48.0 ohms	-	-12	typ	+12	%

Ioz	Output leakage current	-	-5	-	+5	uA
Vihdq(AC)	AC input high	-	Vref+0.175	-		V
Vildq(AC)	AC input low	-	-	-	Vref-0.175	V
Vihdq(DC)	DC input high	-	Vref+0.1	-	VDD	V
Vildq(DC)	DC input low	-	VSS	-	Vref-0.1	V
Vrefdq	ODT enable	-	-	0.5 * Vddq for DDR3 and middle of pad voltage for DDR4	-	V

5.11 Serdes Interface Characteristics

5.11.1 Receive Direction Characteristics

Table 5-19 Receive Input Eye Diagram Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
V RX-DIFF-PKPK	Receiver input differential peak-to-peak voltage	Closed eye	-	**2000**	mV diff-pkpk
V RX-CM-DC	Receiver input DC common-mode voltage	-	0	-	mV
V RX-CM-AC	Receiver Input AC common-mode voltage	-150	-	150	mV pkpk
T RX-DDJ	Receive input signal data dependent Jitter (Inter-symbol interference)	-	-	1	UI pkpk
T RX-RJ	Receive input random jitter	-	-	0.3	UI pkpk
T RX-PJ	Receive input period jitter (At high frequency)	-	-	0.1	UI pkpk
T RX-TJ	Receive input Total Jitter (DDJ + RJ + PJ).	-	-	1	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-pass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to the data rate	-	1667	-	F BAUD /F GPLL

Table 5-20 Receive Loop Loss

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Receiver differential DC return loss	-	-	**-20**	dB
Z RL-DIFF-NYQ	Receiver differential return loss at 5.0 GHz	-	-	-2.5	dB
Z RL-CM-DC	Receiver common-mode DC return loss	-	-	-10	dB
Z RL-CM-NYQ	Receiver common-mode return loss at 5.0 GHz	-	-	-5	dB

Table 5-21 Receive DC Resistance

Parameter	Description	Min.	Typ.	Max.	Units
R DIFF-DC	DC differential receive impedance	80	100	**110**	Ω
R CM-DC	DC common-mode receive impedance	20	25	**27.5**	Ω
R DIFF-HIZ-POS	Differential receive high-impedance for input voltage from 0 V to 200 mV	200k	-	**-**	Ω
R CM-HIZ-POS	Common-mode receive high-impedance for input voltage from 0 V to 200 mV	20k	-	**-**	Ω
R DIFF-HIZ-NEG	Differential receive high-impedance for input voltage from -150 mV to 0 mV	4k	-	**-**	Ω
R CM-HIZ-NEG	Common-mode receive high-impedance for input voltage from -150 mV to 0 mV	1k	-	**-**	Ω

Table 5-22 Received Signal Detection

Parameter	Description	Min.	Typ.	Max.	Units
V IDLE-THRESH	Receiver signal detect input voltage threshold	75	120	**175**	mV diff-pkpk
T SIGDET-ATTACK	Signal detect valid signal attack time (Turn-on time) in SATA mode	-	-	**15**	ns
T SIGDET-DECAY	Signal detect valid signal decay time (Turn-off time) in SATA mode	-	-	**15**	ns
T SIGDET-ATT-DECAYMIS	Signal detect attack/decay time mismatch in SATA mode	-	-	**5**	ns

5.11.2 Transmit Direction Characteristics

Table 5-23 Output Eye Diagram Characteristics

Parameter	Description	Min.	Typ.	Max.	Units

V TX-DIFF-PKPK	Backporch transmit amplitude	400	-	1400	mV diff-pkpk
V TX-EYE-PKPK	Transmit eye voltage opening	400	-	1200	mV diff-pkpk
D TX-N+1-DEEMP	N+1 precursor tap De-emphasis	0	-	5.0	dB
D TX-N-1-DEEMP	N-1 postcursor tap De-emphasis	0	-	8.5	dB
D TX-N-2-DEEMP	N-2 postcursor tap De-emphasis	0	-	2.0	dB
T TX-SLEW	Rise/Fall time	30	-	120	ps
T TX-PJ	Transmit periodic jitter Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	0.05	UI pkpk
T TX-RJ	Transmit total peak-to-peak random jitter (Assumes 14 TXRJ-RMS) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	0.15	UI pkpk
T TX-TJ	Transmit total peak-to-peak jitter (Assumes T TX - TJ = T TX-DDJ + T TX-PJ + T TX-RJ) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	**0.25**	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-sass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to the data rate	-	1667	**-**	F BAUD / F GPLL
V TX-CM-PKPK-AC	AC common-mode voltage variation (Peak-to- peak) at PCIe Gen2 rate	-	-	**100**	mV
V TX-CM-RMS-AC	AC common-mode voltage variation (RMS) at PCIe Gen1 rate	-	-	**20**	mV

Table 5-24 Transmit DC Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
Z TX-DIFF-DC	Transmitter output differential DC impedance	80	100	**120**	Ω

Z TX-CM-DC	Transmitter output common-mode DC impedance	20	25	**30**	Ω
Z TX-DIFF-HIZ	Transmitter output differential DC impedance in squelch mode	-	-	**>2k**	Ω
Z TX-CM-HIZ	Transmitter output common-mode DC impedance in squelch mode	-	-	**> 500**	Ω

Table 5-25 Transmit Loop Loss

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Transmitter differential DC return loss	-	-	**-20**	dB
Z RL-DIFF-NYQ	Transmitter differential return loss at 5.0 GHz	-	-	**-4**	dB
Z RL-CM-DC	Transmitter common-mode DC return loss	-	-	**-10**	dB
Z RL-CM-NYQ	Transmitter common-mode return loss at 5.0 GHz	-	-	**-5**	dB

Table 5-26 Idle Condition

Parameter	Description	Min.	Typ.	Max.	Units
V TX-IDLE	Idle output voltage	-	-	**20**	mV pkpk
V CM-DELTA-SQUELCH	Maximum common-mode step entering/exiting squelch mode	-	-	**50**	mV
T TX-IDLE-LATENCY	Latency entering/exiting idle	-	-	**8**	ns

Table 5-27 Receive Detection

Parameter	Description	Min.	Typ.	Max.	Units
V TX-RCV-DETECT	Voltage change allowed during receiver detection	-	-	**600**	mV

5.12 GEPHY Interface Characteristics

Table 5-28 AC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Units
AC Characteristics						
-	Reference frequency	-	25-0.005%	25	25+0.005%	MHz
-	Reference clock duty cycle	-	40	50	60	%
I_ASICIN_OBD jitter1	Period jitter of the clock from ASIC instead of from	-	-	-	80	ps

	external crystal					
I_ASICIN_OBD jitter2	Cycle-to-cycle jitter of the clock from ASIC instead of from external crystal	-	-	-	120	ps
I_ASICIN_OBD jitter3	Long-term jitter of the clock from ASIC instead of from external crystal (set the trigger delay to 10us)	-	-	-	160	ps
Transmitter char						
2 x Vtxa	Peak-to-peak differential output voltage	10BASE-Te mode	3.08	3.5	3.92	V
2 x Vtxa	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2.0	2.1	V
2 x Vtxa	Peak-to-peak differential output voltage	1000BASE-T mode	-	2.0	-	V
Tr/Tf	Signal rise/fall time	100BASE-TX mode	3.0	4.0	5.0	ns
-	Output jitter	100BASE-TX mode Scrambled idle signal	-	-	1.4	ns
Vtxa	Overshoot	100BASE-TX mode	-	-	5.0	%
Receiver char						
-	Error-free cable length	-	100	-	-	meter

5.13 PCIE2.0 Interface Characteristics

Table 5-29 PCIE Interface Signal Characteristics

Parameter	Description	Min.	Typ.	Max.	Units
VIN	Differential input voltage	120	-	1000	mVpdd
VRIN	Differential input impedance	80	100	120	Ω
VOD	Differential output voltage	800	-	1200	mVpdd

VROUT	Differential output impedance	80	100	120	Ω

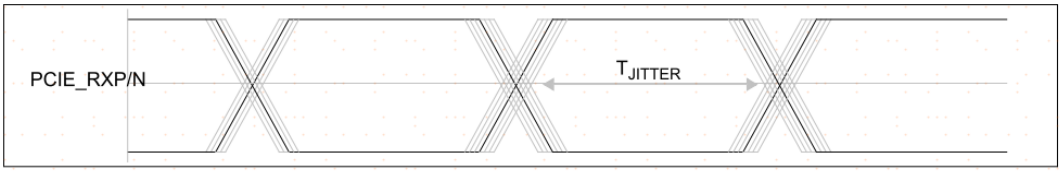


Figure 5-8 PCIE RX Timing

Table 5-30 RX Receive Characteristic

Parameter	Description	Min.	Typ.	Max.	Units
FREQ	Baud Rate	-	2.5/5.0	-	Gbaud
RIN	Input Impedance (Differential)	80	100	120	Ω
VID	Input Voltage (Differential pk-pk)	120	-	1000	mVp-p
TJ	Jitter Tolerance (Min Rx EYE width)	0.4	-	-	Ω

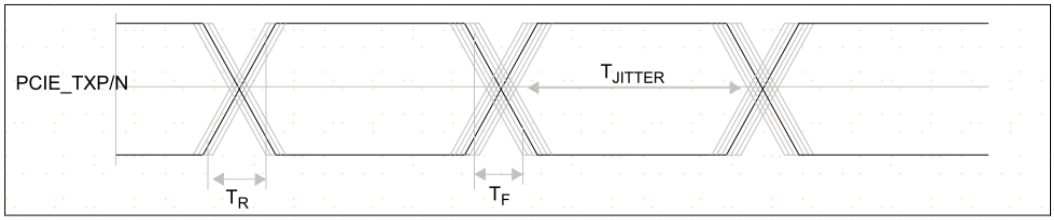


Figure 5-9 PCIE TX Timing

Table 5-31 RX Transmitter Characteristic

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FREQ	Baud Rate			2.5/5.0	-	Gbaud
ROUT	Output Impedance (Differential)		80	100	120	Ω
VOD	Output Voltage (Differential pk-pk)		800	1000	1200	mVp-p
TR/TF	Output Rise/Fall Time (20%~80%)		0.125	-	-	UI
VOEQ	Output De-Emphasis	Gen1 2.5 Gbps Gen2 5.0 Gbps	-3.0 -5.5	-3.5 -6.0	-4.0 -6.5	dB
TR/TF	Rise/Fall Time (20%–80%)	Gen1 2.5 Gbps Gen2 5.0 Gbps	0.125 0.150	- -	- -	ns
TJ	Jitter (min Tx EYE width)		0.75	-	-	UI

6 Clock Input Requirements

The chip requires an external input of 25Mhz clock. Passive crystal oscillator circuit or active crystal oscillator can be used. The input 25MHz clock has the following requirements:

Table 6-1

Symbol	Description	Min.	Typ.	Max.	Units
VIH	Input high voltage	2.0	--	--	V
VIL	Input low voltage			0.8	V
Tfrequency	Clock frequency		25		MHz
Δfrequency	Clock tolerance	-50	-	50	ppm
C1	Load cap	12		27	pF
C2	Load cap	12		27	pF
Tdc	Duty cycle		50%		%

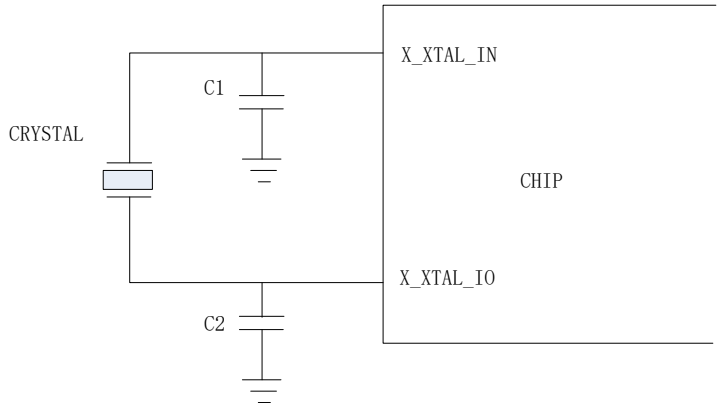


Figure 6-1 Crystal Circuit Diagram

7 Reliability Characteristics

7.1 Reliability Parameters

Table 7-1

Parameter	Max.	Units	Notes
HBM	2K	V	

CDM	250	V	
MM	200	V	
Latch-up	200	mA	
MSL	3	Grade	

7.2 Maximum Working Environment

Table 7-2

Parameter	Symbol	Min.	Max.	Units
Junction temperature limit	Tj	-40	+125	℃

7.3 Recommended Working Environment

Table 7-3

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient temperature	Ta	0	25	70	℃
Welding temperature	Tp	225	235	245	℃
Junction temperature	Tj	-40	-	125	℃
Storage temperature	Ts	-55	-	150	℃
Relative humidity	RH	-	50	90	%

7.4 Thermal Characteristics

Table 7-4 Thermal Resistance

Theta Ja (℃/W)			Psi jt (℃/W)	Theta Jc (℃/W)	Theta Jb (℃/W)
0 m/s	1 m/s	2 m/s			
14.1	12.5	11.9	6.4	8.4	13.0

8 Power Parameters

8.1 Power Consumption

Maximum Power Consumption: 4.50W（Environmental: 70° C）
Typical Power Consumption: 3.70W（Environmental: 25° C）

8.2 MAX Current of Power Branch

Table 8-1

Name	Num	Voltage Value (V)	Range	Noise Tolerance (mV)	MAX Current (mA)	Notes
VCC3IO	10	3.3	±10%	50	260	3.3V digital IO power
VCC33A_GPHY	3	3.3	-5%~+10%	30	329	GPHY 3.3V analog power
USB2VCC33A	1	3.3	-5%~+10%	30	10	USB2 3.3V analog power
USB3VCC33A	1	3.3	-5%~+10%	30	10	USB3 3.3V analog power
VCC18	4	1.8	±10%	30	300	1.8V digital power
VCC18A_PON	9	1.8	-5%~+10%	30	70	PON 1.8V analog power
USB2VCC18A	1	1.8	-5%~+10%	30	40	USB2 1.8V analog power
USB3VCC18A	1	1.8	-5%~+10%	30	59	USB3 1.8V analog power
TDC_VCC18A	1	1.8	-5%~+10%	30	2	Temperature sensor 1.8V analog power
PLL_VCC18A	1	1.8	-5%~+10%	30	30	PLL 1.8V analog power
XTAL_VCC18	1	1.8	±10%	30	2	Crystal1.8V analog power
VDT_VCC18A	1	1.8	-5%~+10%	30	2	VDT 1.8V power
PCIE0_VPH	1	1.8	-5%~+10%	30	35	PCIe0 1.8V power
PCIE1_VPH	1	1.8	-5%~+10%	30	35	PCIe1 1.8V power
DDR_PLLVCCA	1	1.8	-5%~+10%	30	7	1.8V DDR PLL voltage

LDO_VCC18A	2	1.8	-5%~+10%	30	350	Built-in LDO input
LDO_O_VCC12A	2	1.5/1.2	-5%~+10%	30	350	Built-in LDO output
VDDQ	7	1.5/1.2	-5%~+10%	30	200	DDR3/DDR4 IO power,DDR3 is 1.5V and DDR4 is 1.2V
VCC11K	9	1.1	±10%	30	350	GPHY 1.1V supply voltage
VCC11A_GPHY	3	1.1	-5%~+10%	30	450	GPHY 1.1V Analog voltage
VCCK	16	0.9	±10%	30	900	0.9V supply voltage
VCC_VP0	1	0.9	-5%~+10%	30	60	0.9V PCIe0 supply voltage
VCC_VP1	1	0.9	-5%~+10%	30	60	0.9V PCIe1 supply voltage
VCC09A_PON	2	0.9	-5%~+10%	30	80	0.9V PON analog voltage
USB3VCC09A_RX	1	0.9	-5%~+10%	30	12	0.9V USB3 receive supply voltage
USB3VCC09A_TX	1	0.9	-5%~+10%	30	3	0.9V USB3 transmit supply voltage
PLL_VCC	1	0.9	-5%~+10%	30	15	0.9V PLL supply voltage
LVTX_VCC09A	1	0.9	-5%~+10%	30	5	0.9V PCIe reference clock supply voltage

8.3 Power on and Power off Sequence

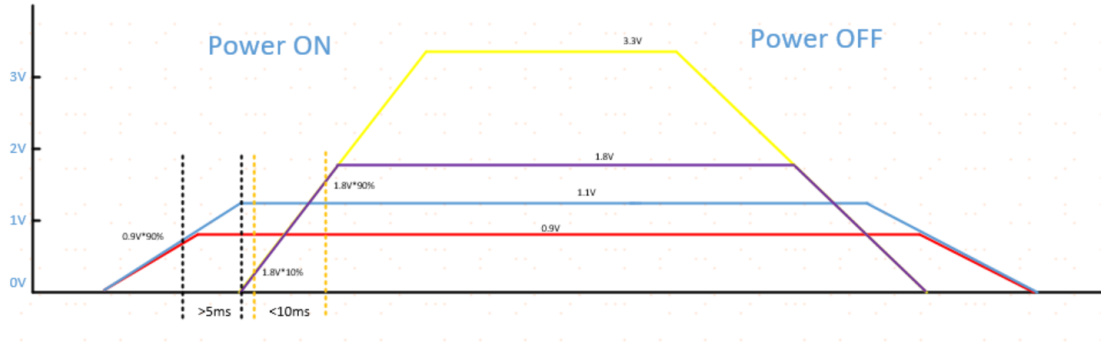


Figure 8-1 Chip Power-on Sequence Diagram

The chip is powered on and powered off according to the following recommended sequence:

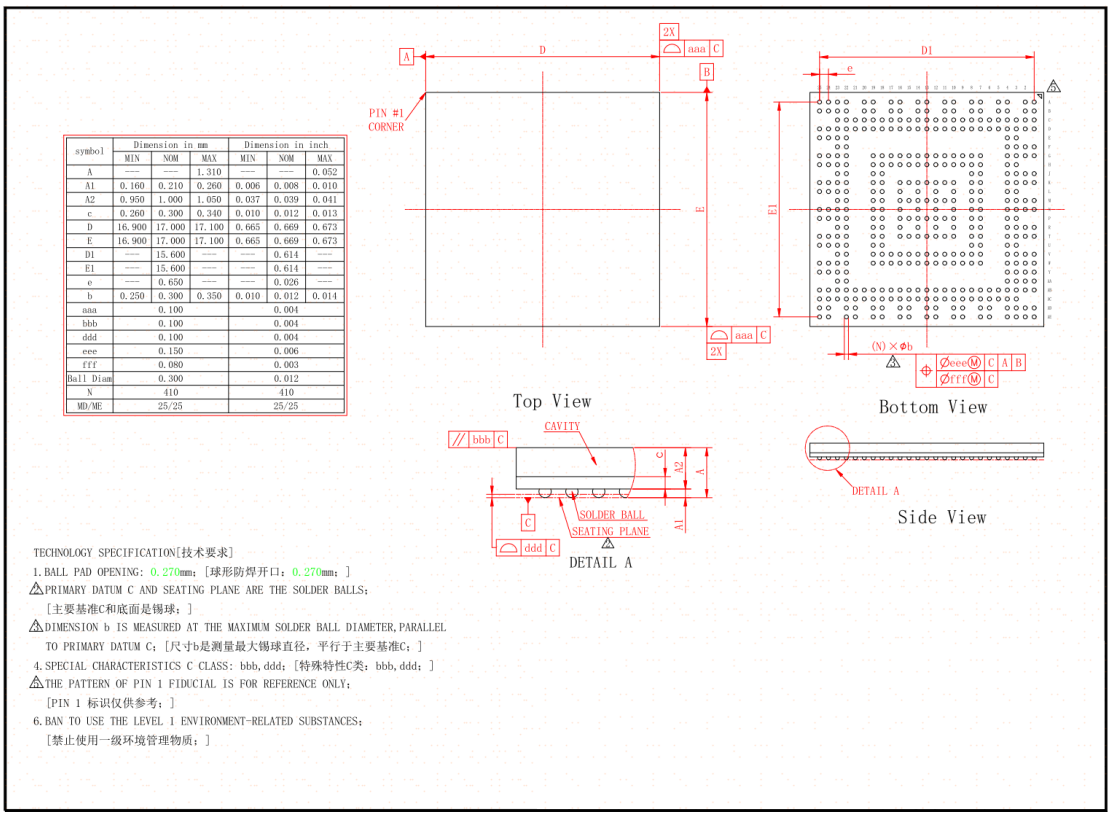
1. Power on 0.9V and 1.1V first, and keep 0.9V for more than 5ms before powering on 1.8 and 3.3V;
2. 0.9V and 1.1V can be powered on at the same time;
3. 1.8V and 3.3V can be powered on at the same time;
4. The 1.8V power-on time should be less than 10ms;
5. Power off 1.8V and 3.3V first, and power off after 0.9V and 1.1V.

8.4 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
I/O ring supply (3.3V) and Analog, reference	VCC3IO,VCC33A (Including all 3.3V supply)	-0.5	4.6	V
I/O ring supply (1.8V) and Analog, reference	VCC18, VCC18A (Including all 1.8V supply)	-0.5	2.5	V
DDR I/O ring supply(1.5V)	VDDQ	-0.4	1.98	V
Analog and digital core logic supply(0.9V)	VCC, VCCK (Including all 0.9V supply)	-0.4	1.05	V
I/O ring supply (1.1V) and Analog, reference	VCC11K, VCC11A (Including all 1.1V supply)	-0.5	1.5	V

9 Mechanical Characteristics

Packaging Characteristics



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	----	----	1.310	----	----	0.052
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.950	1.000	1.050	0.037	0.039	0.041
c	0.260	0.300	0.340	0.010	0.012	0.013
D	16.900	17.000	17.100	0.665	0.669	0.673
E	16.900	17.000	17.100	0.665	0.669	0.673
D1	----	15.600	----	----	0.614	----
E1	----	15.600	----	----	0.614	----
e	----	0.650	----	----	0.026	----
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	410			410		
MD/ME	25/25			25/25		

TECHNOLOGY SPECIFICATION[技术要求]

1. BALL PAD OPENING: 0.270mm; [球形防焊开口：0.270mm；]

⚠PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;

[主要基准C和底面是锡球；]

⚠DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C; [尺寸b是测量最大锡球直径，平行于主要基准C；]

4. SPECIAL CHARACTERISTICS C CLASS: bbb, ddd; [特殊特性C类：bbb, ddd；]

⚠THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;

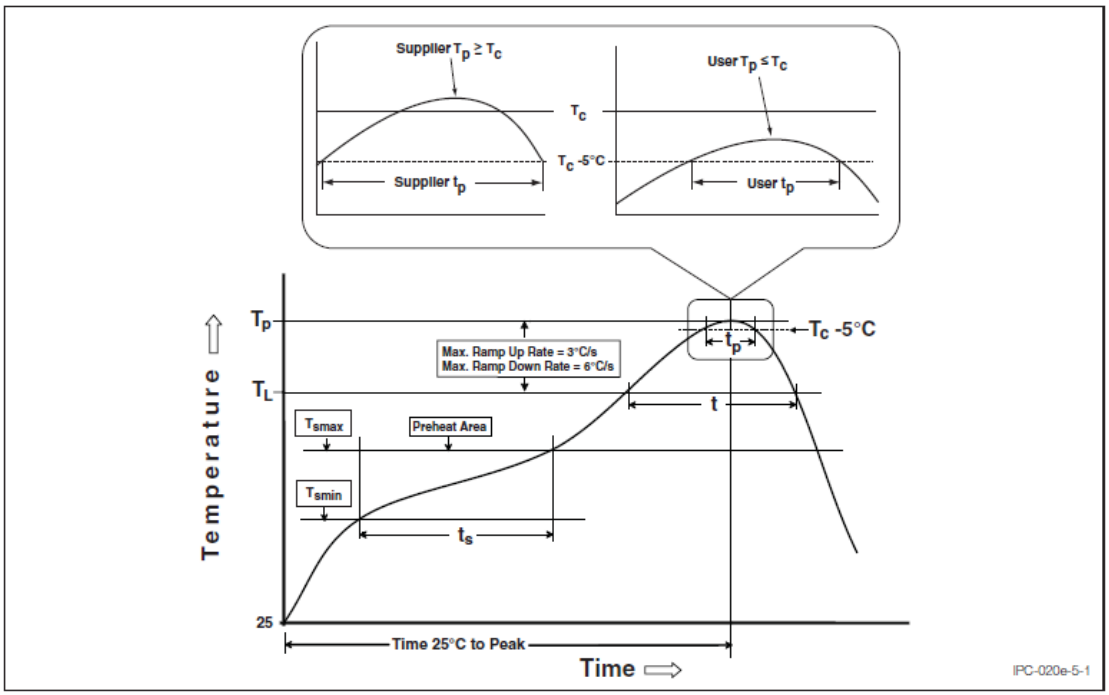
[PIN 1 标识仅供参考；]

6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;

[禁止使用一级环境管理物质；]

Figure 9-1 Packaging Physical Dimensions

10 Reflow Profile



Profile	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat and soak Min. temperature (Ts_{min}) Max. temperature (Ts_{max}) Time (ts_{min} to ts_{max}) (t_s)	 100 °C 150 °C 60 ~ 120 seconds	 150 °C 200 °C 60 ~ 120 seconds
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second (Max.)	3 °C/second (Max.)
Liquid temperature (T_L) Time at liquid (t_L)	183 °C 60 ~ 150 seconds	217 °C 60 ~ 150 seconds
Peak package body temperature (T_p)*	235℃	260℃
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to Ts_{max})	6 °C/second (Max.)	6 °C/second (Max.)
Time to peak temperature from 25 °C	6 minutes (Max.)	8 minutes (Max.)
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		