5VT2510
DATASHEET

Contents

REVISION HISTORY

Version	Date	Author	Change	Remark
V1.0	2020/11/2	Wingston	Initial version	
V1.1	2022/1/6	Wingston	English version	
V1.2	2022/8/1	Wingston	English version supplement	
V1.3	2022/8/31	Wingston	Modify the SPI timing figure and I2C timing figure	

1 OverView

1.1 Chip Introduction

5VT2510 is a highly integrated EPON/GPON Home Gateway system on chip, integrated PON MACs, SerDes,one integrated Gigabit Ethernet PHYs, can provide low-cost solution of home network gateway.

5VT2510 is a single-core processor, could perform processing of Layer 2 and Layer 3 NAT/NAPT packet, also could perform power analyses for different network-protocols, integrates packet hardware accelerator based on IP/port/vlan/network protocol, which could accelerate lots of protocols packets, such as :VLAN, SNAP/LLC, PPPoE, IP, TCP, UDP, ICMP, IGMP, DHCP, and HTTP.

5VT2510 already integrates DDR1 memory.

Feartures

- System Processo
  533MHz CPU，ARMV5 processor
  I-Cache: 32KB
  D-Cache: 32KB
- Flash Interface
  SPI NOR Flash
  Maximum size 512Mb
- 2 I2C interface
- UART interface
- GPON
  ---Compliant with ITU-T G.984.x GPON
  Supports data rates of 1.24416Gps upstream/2.48832Gbps downstream
  Supports AES, key switching of downstream
  Supports FEC of upstream/downstream
  Supports dying gasp
- EPON
  ---Compliant with IEEE 802.3 EPON MAC standard
  Supports data rates of 1.25Gbps upstream/1.25Gbps downstream
  Supports FEC of upstream/downstream
  Supports encryption downstream
  Supports dying gasp
- Layer 2/layer 3 packet hardware accelerator for NAT/NAPT
  Support up to32K NAPT rules /4K NAPTR rules
  Support IPv4/IPv6 protocols
  Layer 2 traffic based on VLAN, or could based on IP and port
  Layer 3 traffic based on IP and port
  Support IPoE/DHCP/PPPoE WAN hardware packet accelerator

Support DS-Lite multicast

- Support ACL(access control list)

  Based on MAC, IP, TCP/UDP, ICMP,IGMP, IPv6

  Support actions of mirror, redirect, dropping,

  Supporting queuing and scheduling, traffic monitoring

  Support packet length/VID/IP/L4 Port range check
- Support IEEE 802.1Q VLAN

  Support up to 4K VLANs

  Support Untag definition in each VLAN

  Supports VLAN based on port and protocol
- Support Quality of Service (QoS)
- Single 25MHz reference crystal or oscillator
- 10x10mm QFN 88-pin package

1.2 Block Diagram

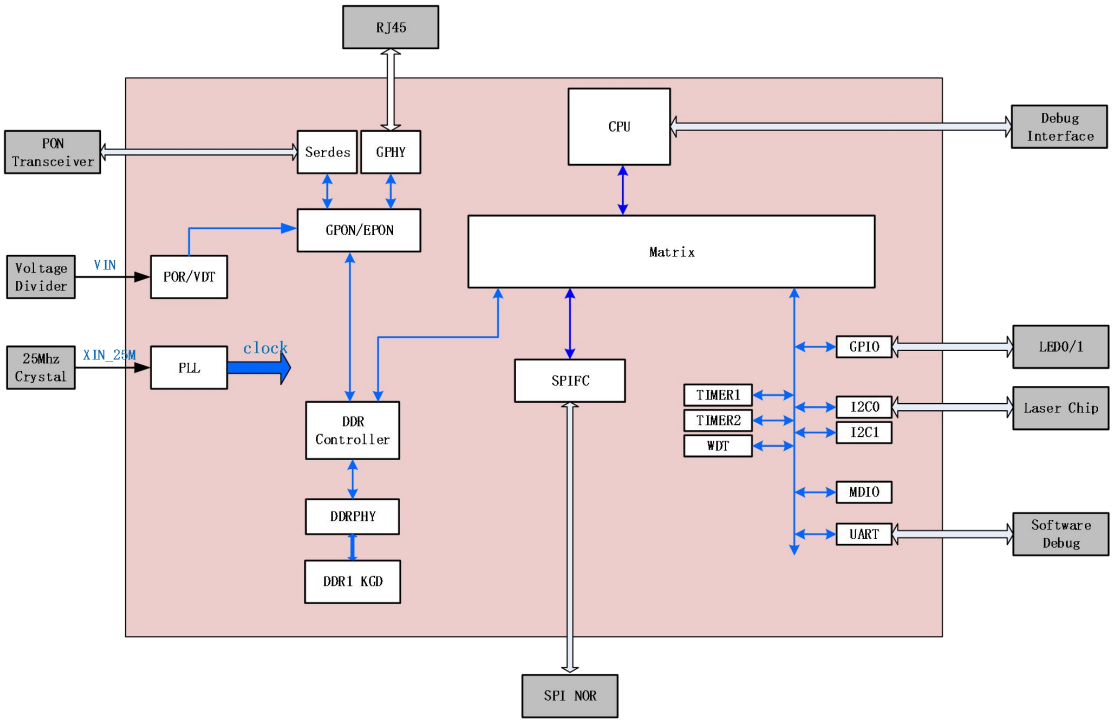


Figure 1 Embedded DDR1 KGD

Remark： Bot I2C0 and I2C1 can be used in optical module， they are no different.

2 Balls

2.1 Ball Map

Ball Map of Embedded DDR1 KDG

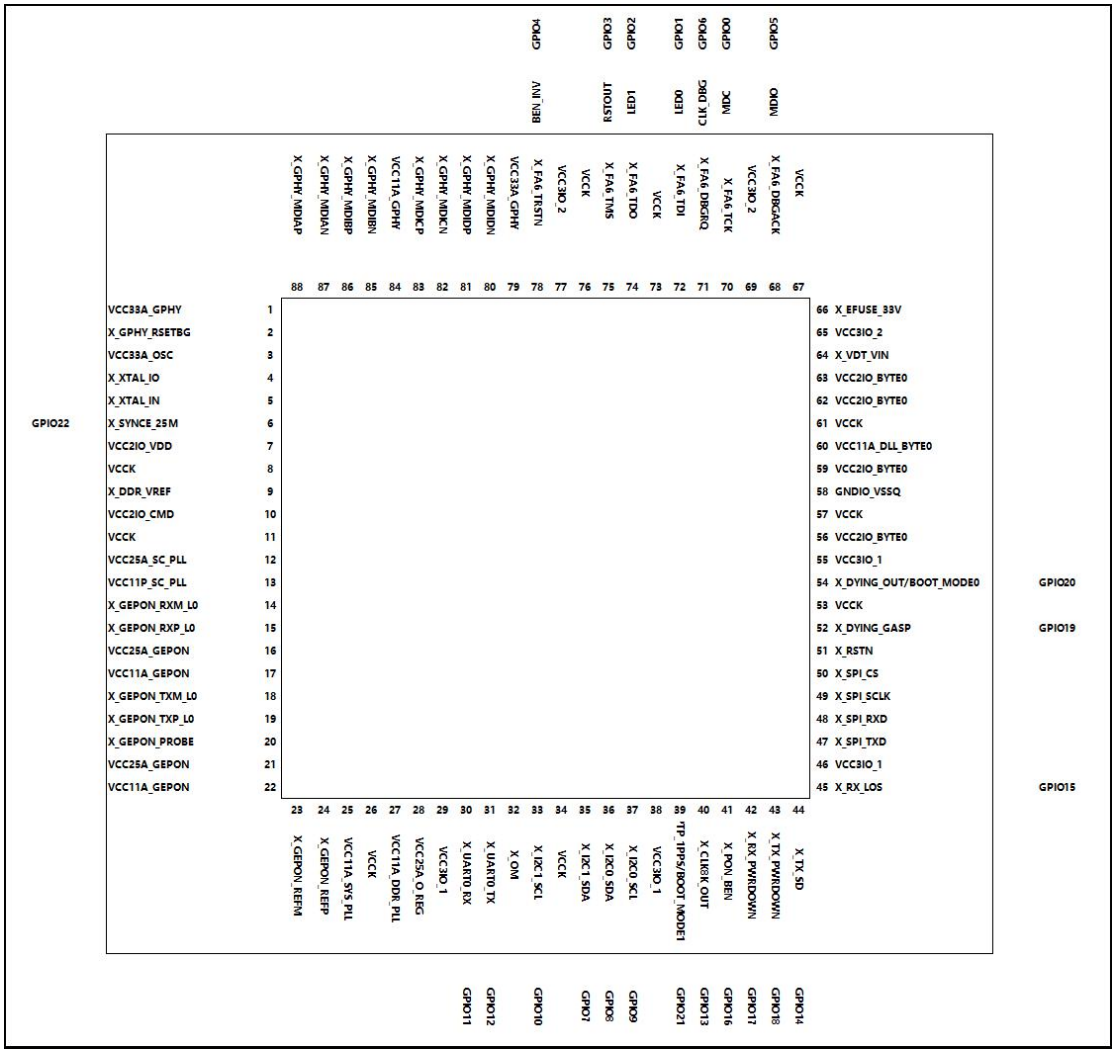


Figure 2 5VT2510 Ball Map

2.2 Balls Description

AI ： Analog input

AIO ： Analog input/output

AO ： Analog output
IT ： Input，TTL compatible
OT ： Tristate output，TTL compatible
ITOT： Input/Output，TTL compatible
PG ： Power Ground

Table 1

Pin	Name	IO Type	Default Value	Description
1	VCC33A_GPHY	PG		GPHY3.3V analog power,bead required, PIN79 and PIN1 use same bead
2	X_GPHY_RSETBG	AI		GEPHY analog circuit reference voltage，connect this pin to ground though a 3KΩ±1% resistor.
3	VCC33A_OSC	PG		Crystal IO 3.3V power，combined with nearby digital power
4	X_XTAL_IO	AIO		Crystal IO output，connect a 25MHZ crystal
5	X_XTAL_IN	AI		Crystal IO input，connect a 25MHZ crystal at this input，if oscillator, only need connect to this pin. External Crystal circuit,C1/C2 must between 12pf~27pf，frequency stability must be within ±50ppm.
6	X_SYNCE_25M	ITOT	Pull down	Could input 25Mhz clock in SyncE function. 25Mhz clock is generated from external PLL with 8KHz clock and sent to GEPHY，OLT and GEPHY have same source clock. Normally used as SyncE pin, if not,this pin could be used as GPIO
7	VCC2IO_VDD	PG		DDR 2.5V power，connected directly to digital power
8	VCCK	PG		Core1.1V power，connected directly to digital power
9	X_DDR_VREF	PG		The reference voltage of DDRPHY is 1/2 component voltage of DDR 2.5V power supply, 0.5 * VCC2IO_CMD.
10	VCC2IO_CMD	PG		DDR 2.5V power，connected directly to digital power
11	VCCK	PG		Core 1.1V power，connected directly to digital power
12	VCC25A_SC_PLL	PG		PLL 2.5V analog power,bead required，PIN12 PIN16 and PIN21 use same bead
13	VCC11P_SC_PLL	PG		PLL 1.1V analog power,bead required，Note：Independent bead required

14	X_GEPON_RXM_L0	AI		Serdes RX differential signal negative,can not reverse pair,AC coupled
15	X_GEPON_RXP_L0	AI		Serdes RX differential signal positive,can not reverse pair,AC coupled
16	VCC25A_GEPON	PG		Serdes 2.5V analog power，bead required，PIN12 PIN16 and PIN21 use same bead
17	VCC11A_GEPON	PG		Serdes 1.1V analog power，bead required，PIN17 and PIN22 use same bead
18	X_GEPON_TXM_L0	AO		Serdes TX differential signal negative,can not reverse pair,AC coupled
19	X_GEPON_TXP_L0	AO		Serdes TX differential signal positive,can not reverse pair,AC coupled
20	X_GEPON_PROBE	AO		Serdes probe Pin,left unconnected if not be used.
21	VCC25A_GEPON	PG		Serdes 2.5V analog power,bead required,PIN12 PIN16 and PIN21 use same bead
22	VCC11A_GEPON	PG		Serdes 1.1V analog power,bead required,PIN17 and PIN22 use same bead
23	X_GEPON_REFM	AI		Serdes reference clock input backup pin,left unconnected
24	X_GEPON_REFP	AI		Serdes reference clock input backup pin，left unconnected
25	VCC11A_SYS_PLL	PG		PLL 1.1V analog power,bead required,PIN27 and PIN25 use same bead
26	VCCK	PG		Core 1.1V power，connected directly to digital power
27	VCC11A_DDR_PLL	PG		DDR internal PLL 1.1V analog power,bead required,PIN27 and PIN25 use same bead
28	VCC25A_O_REG	PG		Internal LDO provide 2.5V power,external >=3.3uf capacitor required, provide power for PLL and SerDes,connect PIN12 PIN16 PIN21 and PIN28 in PCB
29	VCC3IO_1	PG		Directly connect to the power supply after the coalescence between IO 3.3V power supply and internal LDO 3.3V input power supply. Additionally, a 47uF filter capacitor is required
30	X_UART0_RX	ITOT	None	UART RX input，GPIO multiplexed
31	X_UART0_TX	ITOT	None	UART TX output，GPIO multiplexed
32	X_OM	IT	Pull down	Chip test mode Pin,internal pull-down resistor by default 0:chip normal working mode 1:chip test mode

				Connect this pin to ground when chip normally works
33	X_I2C1_SCL	ITOT	Pull up	I2C0 clock，as I2C,pull-up resistor required; I2C1 is the same with I2C0，GPIO multiplexed
34	VCCK	PG		Core 1.1V power，connected directly to digital power
35	X_I2C1_SDA	ITOT	Pull up	I2C1 data，as I2C,pull-up resistor required;I2C1 is the same with I2C0，GPIO multiplexed
36	X_I2C0_SDA	ITOT	Pull up	I2C0 data，as I2C,pull-up resistor required;I2C1 is the same with I2C0，GPIO multiplexed
37	X_I2C0_SCL	ITOT	Pull up	I2C0 clock，as I2C,pull-up resistor required;I2C1 is the same with I2C0，GPIO multiplexed
38	VCC3IO_1	PG		IO 3.3V power，connected directly to digital power
39	X_PTP_1PPS/BOOT_MODE1	ITOT	None	It is used to output 1ps pulse signal and is also the pin for boot modes: Boot_ Mode1, the level state of the sampled signal when power on reset 0: ROM boot for normal operation 1: XIP SPINOR boot for standby mode This multiplexed GPIO function
40	X_CLK8K_OUT	ITOT	None	Could input 8Khz clock in SyncE function. 25Mhz clock is generated from external PLL with 8KHz clock and sent to GEPHY，OLT and GEPHY have same source clock. Normally used as SyncE pin, if not,this pin could be used as GPIO
41	X_PON_BEN	ITOT	None	PON Burst enable 1:Disable(Default voltage after power up) 0:Enable Can configure polarity of voltage; This pin is also GPIO multiplexed
42	X_RX_PWRDOWN	ITOT	Pull down	Disable PON receive; high-level output voltage,enable PON receive, low-level output voltage,disable PON receive; GPIO multiplexed
43	X_TX_PWRDOWN	ITOT	Pull up	Disable PON transmit; high-level output voltage,disable PON transmit,

				low-level output voltage,enable PON transmit; GPIO multiplexed
44	X_TX_SD	ITOT	None	Detect PON transmitted signal,GPIO multiplexed
45	X_RX_LOS	ITOT	None	Detect PON received signal，GPIO multiplexed
46	VCC3IO_1	PG		IO 3.3V power，connected directly to digital power
47	X_SPI_TXD	OT	None	SPI NOR receive data signal
48	X_SPI_RXD	IT	None	SPI NOR transmit data signal
49	X_SPI_SCLK	OT	None	SPI NOR clock signal
50	X_SPI_CS	OT	None	SPI NOR chip selection
51	X_RSTN	IT	Pull up	The reset input of the chip needs a built-in Schmidt input mode or it can realize a 3.3V high level fixing. During the process, a resistance capacitance reset circuit is a good choice.
52	X_DYING_GASP	ITOT	Pull down	Dying_gasp input backup pin,chip already have internal dying gasp circuitry,if use external dying-gasp circuitry,this pin could be input pin; GPIO multiplexed
53	VCCK	PG		Core 1.1V power，connected directly to digital power
54	X_DYING_OUT/BOOT_MODE0	ITOT	Pull down	Dying_out is designed to output the internal VDT detection results to off chip for other control purposes. boot_ mode0, the level state of the sampled signal when the chip is in the state of power-on reset. 0:uart boot 1:spinor boot This multiplexed GPIO function
55	VCC3IO_1	PG		IO 3.3V power,connected directly to digital power
56	VCC2IO_BYTE0	PG		DDR 2.5V power,connected directly to digital power
57	VCCK	PG		Core 1.1V power,connected directly to digital power
58	GNDIO_VSSQ	PG		DDR power ground,connected directly to board-level power
59	VCC2IO_BYTE0	PG		DDR 2.5V power，connected directly to digital power

60	VCC11A_DLL_BYTE0	PG		DDR DLL 1.1V analog power,bead required,
61	VCCK	PG		Core 1.1V power，connected directly to digital power
62	VCC2IO_BYTE0	PG		DDR 2.5V power，connected directly to digital power
63	VCC2IO_BYTE0	PG		DDR 2.5V power，connected directly to digital power
64	X_VDT_VIN	AI		Connect the component voltage divider resistance network of 12V power supply to provide 1.22V reference voltage for monitoring 12V power failure. If it fails to a certain voltage (9.6~10.1v), the component voltage divider resistance network will get a voltage lower than 1.22V, and at this point, ONU chip will report a signal to OLT dying_ gasp.
65	VCC3IO_2	PG		IO 3.3V power，connected directly to digital power
66	X_EFUSE_33V	PG		During eFUSE generation test, the programming needs a 3.3V power supply, and the chip is suspended when operates normally.
67	VCCK	PG		Core 1.1V power，connected directly to digital power
68	X_FA6_DBGACK	ITOT	None	The default function is the debug ack pin output by the processor, connected to an external ICE emulator, multiplexing the MDIO function and the GPIO function
69	VCC3IO_2	PG		IO 3.3V power，connected directly to digital power
70	X_FA6_TCK	ITOT	Pull down	JTAG Clock(Default); MDC multiplexed，be used to send MDIO clock to external PHY; GPIO multiplexed
71	X_FA6_DBGRQ	ITOT	Pull down	The default function is the debugging request signal sent by the external ICE simulator to the internal processor. During its boot process, the chip needs to be connected to the low level. After booting, the electrical level needn’t stay low by switching to GPIO and other functions through the configuration register. The multiplexed CLK_DBG function is used to output some specific clocks for locating

				problems.
72	X_FA6_TDI	ITOT	Pull up	JTAG Serial Data In(Default), LED0 multiplexed; GPIO multiplexed
73	VCCK	PG		Core 1.1V power，connected directly to digital power
74	X_FA6_TDO	ITOT	None	JTAG Serial Data Out(Default); LED1 multiplexed; GPIO multiplexed
75	X_FA6_TMS	ITOT	Pull up	JTAG Test Mode Select(Default); RST_OUT multiplexed,could be used to send chip internal reset signal to external component; GPIO multiplexed
76	VCCK	PG		Core 1.1V power，connected directly to digital power
77	VCC3IO_2	PG		IO 3.3V power,connected directly to digital power
78	X_FA6_TRSTN	ITOT	Pull down	JTAG Test Reset(Default); PON_BEN_INV multiplexed,can be used as PON_BEN inverted signal，normally not be used; GPIO multiplexed This signal should be tied to ground via pull-down resistor if not use it.
79	VCC33A_GPHY	PG		GEPHY 3.3V analog power,bead required,PIN79 and PIN1 user same bead
80	X_GPHY_MDIDN	AIO		GEPHY pair D differential signal negative, can reverse pair,support A->B, B->A, C->D, D->C
81	X_GPHY_MDIDP	AIO		GEPHY pair D differential signal positive, can reverse pair,support A->B, B->A, C->D, D->C
82	X_GPHY_MDICN	AIO		GEPHY pair C differential signal negative, can reverse pair,support A->B, B->A, C->D, D->C
83	X_GPHY_MDICP	AIO		GEPHY pair C differential signal positive, can reverse pair,support A->B, B->A, C->D, D->C
84	VCC11A_GPHY	PG		GEPHY 1.1V analog power,bead required,
85	X_GPHY_MDIBN	AIO		GEPHY pair B differential signal negative, can reverse pair,support A->B, B->A, C->D, D->C
86	X_GPHY_MDIBP	AIO		GEPHY pair B differential signal positive，can reverse pair,support A->B, B->A, C->D, D->C
87	X_GPHY_MDIAN	AIO		GEPHY pair A differential signal negative, can reverse pair,support A->B, B->A, C->D, D->C
88	X_GPHY_MDIAP	AIO		GEPHY pair A differential signal positive, can reverse pair,support A->B, B->A, C->D, D->C

Note：Internal pull up/down by connecting pin to ground through 75KΩ resistor

2.3 Pin Sharing Schemes

Table 2:GPIO Multiplexed Pin Options

Pin	Name	Default Function		2nd Function		3rd Function	
		Name	Direction	Name	Direction	Name	Direction
6	X_SYNCE_25M	X_SYNCE_25M	IN	GPIO22	INOUT		
30	X_UART0_RX	X_UART0_RX	IN	GPIO11	INOUT		
31	X_UART0_TX	X_UART0_TX	OUT	GPIO12	INOUT		
33	X_I2C1_SCL	X_I2C1_SCL	INOUT	GPIO10	INOUT		
35	X_I2C1_SDA	X_I2C1_SDA	INOUT	GPIO7	INOUT		
36	X_I2C0_SDA	X_I2C0_SDA	INOUT	GPIO8	INOUT		
37	X_I2C0_SCL	X_I2C0_SCL	INOUT	GPIO9	INOUT		
39	X_PTP_1PPS	X_PTP_1PPS	OUT	GPIO21	INOUT		
40	X_CLK8K_OUT	X_CLK8K_OUT	OUT	GPIO13	INOUT		
41	X_PON_BEN	X_PON_BEN	OUT	GPIO16	INOUT		
42	X_RX_PWRDOWN	X_RX_PWRDOWN	OUT	GPIO17	INOUT		
43	X_TX_PWRDOWN	X_TX_PWRDOWN	OUT	GPIO18	INOUT		
44	X_TX_SD	X_TX_SD	IN	GPIO14	INOUT		
45	X_RX_LOS	X_RX_LOS	IN	GPIO15	INOUT		
52	X_DYING_GASP	X_DYING_GASP	IN	GPIO19	INOUT		
54	X_DYING_OUT	X_DYING_OUT	OUT	GPIO20	INOUT		
68	X_FA6_DBGACK	X_FA6_DBGACK	OUT	GPIO5	INOUT	MDIO	INOUT
70	X_FA6_TCK	X_FA6_TCK	IN	GPIO0	INOUT	MDC	OUT
71	X_FA6_DBGRQ	X_FA6_DBGRQ	IN	GPIO6	INOUT	CLK_DBG	OUT
72	X_FA6_TDI	X_FA6_TDI	IN	GPIO1	INOUT	LED0	OUT
74	X_FA6_TDO	X_FA6_TDO	OUT	GPIO2	INOUT	LED1	OUT
75	X_FA6_TMS	X_FA6_TMS	IN	GPIO3	INOUT	RST_OUT	OUT
78	X_FA6_TRSTN	X_FA6_TRSTN	IN	GPIO4	INOUT	PON_BEN_INV	OUT

3 Features Description

3.1 SOC Subsystem

3.1.1 CPU

RISC-32bit embeded CPU，533Mhz ARM V5TE ® architecture-compatible processor.

3.1.2 DDR

Embedded 256Mb DDR1，up to 400Mbps data rate.

3.1.3 SPINOR

Supports peripheral SPI NOR component，up to 50Mhz clock rate，up to 512Mb size.

3.2 ONU Subsystem

Supports ITU-T GPON G.984/G.988 and IEEE802.3 EPON standards；
Support Layer 2/layer 3 packet hardware accelerator for NAT/NAPT；
Support 1Gbps Ethernet interface；
Supports DDR1/DDR2 memory；
Supports QOS;
Analyse lots of protocols packets, such as :PPPoE/IP/TCP/UDP/ICMP/IGMP

4 Interface Characteristics

4.1 SPI NOR Controller Interface Timing

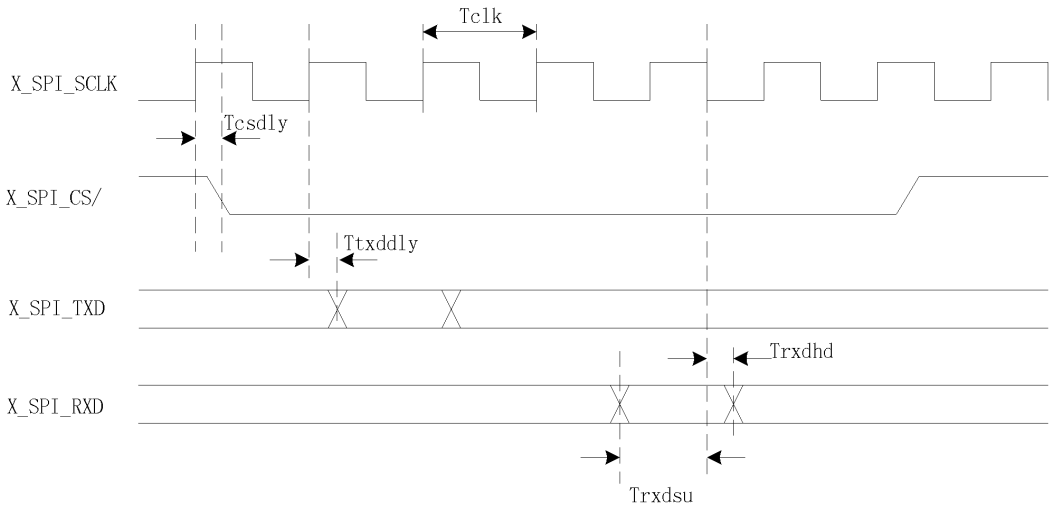


Figure 3 SPI NOR interface Timing

Table 5

Description	Symbol	Min.	Typ.	Max.	Units
X_SPI_SCLK clock cycle	Tclk	20	40	-	ns
Setup time for input	Trxdsu	10	-	-	ns
Hold time for input	Trxdhd	2	-	10	ns
Delay time for output @50Mhz,15pF	Ttxddly Tcsdly	-	-	8	ns

Note: The receiving direction uses the falling edge to sample the data.

4.2 JTAG Interface Timing

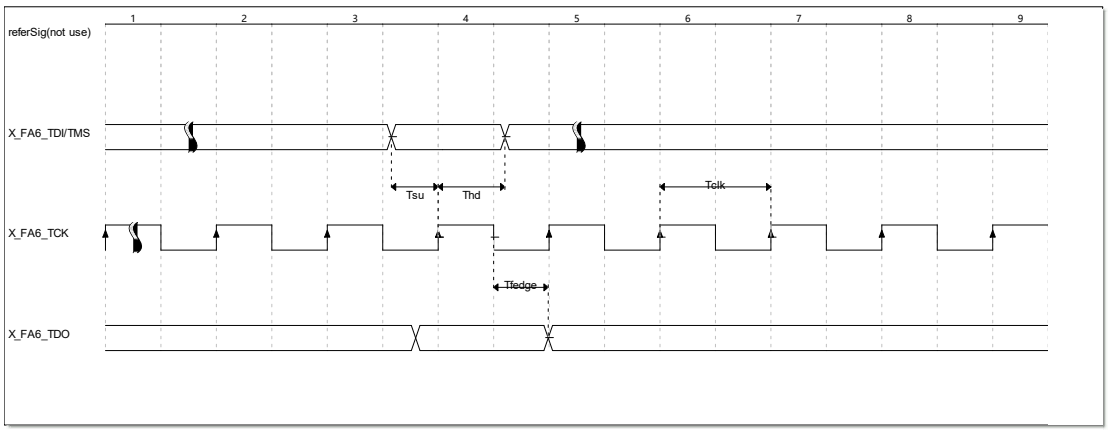


Figure 4 JTAG interface timing

Table 6

Description	Symbol	Min.	Typ.	Max.	Units

X_FA6_TCK clock cycle	Tclk	100	200	-	ns
Setup time for input	Tsu	10	-	-	ns
Hold time for input	Thd	10	-	-	ns
Delay time for output	Tdly	-		20	ns

4.3 MDIO Interface Timing

Receive：

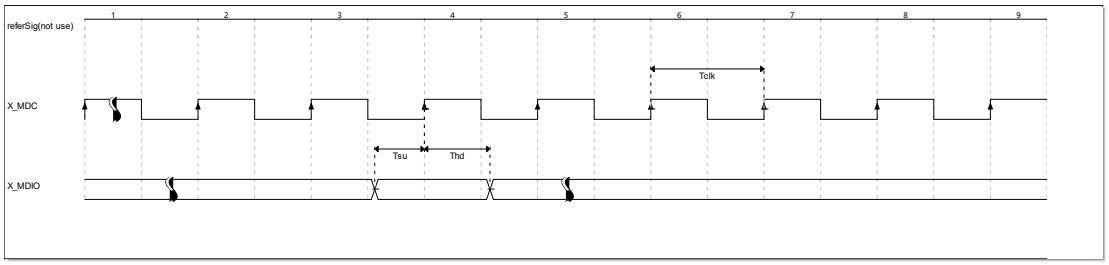


Figure 5 MDIO Interface Receive Timing

Transmit:

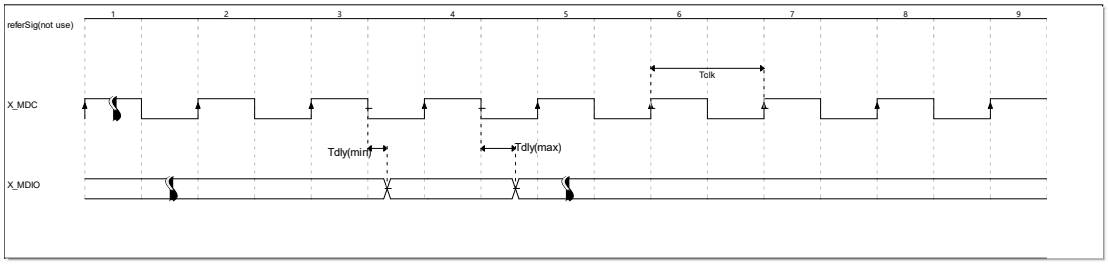


Figure 6 MDIO Interface Transmit Timing

Table 7

Description	Symbol	Minx	Typ.	Max.	Units
MDC clock cycle	Tclk	2500	2000	-	ns
Setup time for input	Tsu	10	-	-	ns
Hold time for input	Thd	10	-	-	ns
Delay time for output	Tdly	--		1000	ns

4.4 I2C Interface Timing

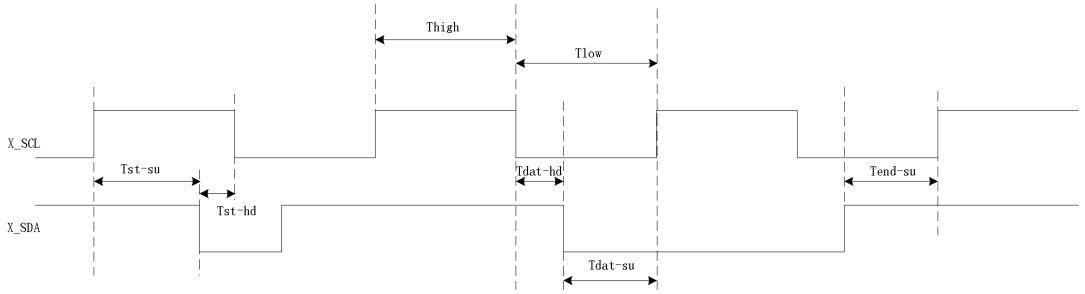


Table 7 I2C Interface Timing

Table 8

Symbol	Name	Standard mode		Fast mode		Units
		Min.	Max.	Min.	Max.	
fscl	Clock frequency		100		400	Khz
Tlow	Clock low-level voltage time	4.7		1.3		us
Thigh	Clock high-level voltage time	4.0		0.6		us
Tst-su	Setup time for start	4.7		0.6		us
Tst-hd	hold time for start	4.0		0.6		us
Tdat-su	Setup time for data	250		100		ns
Tdat-hd	Hold time for data	5.0	3.45	0	0.9	us
Tend-su	Setup time for end	4.0		0.6		us

Note：Tdat-hd uses the Max value(3.45us) only when the SCL Tlow is not extended.

4.5 SerDes Interface Parameters

4.5.1 Receive Direction Parameters

Receive Input Eye Diagram CharacteristicsTable 9

Parameter	Description	Min.	Typ.	Max.	Units
V RX-DIFF-PKPK	Receiver input differential peak-to-peak voltage	Closed eye	-	**2000**	mV diff-pkpk
V RX-CM-DC	Receiver input DC common-mode voltage	-	0	-	mV
V RX-CM-AC	Receiver Input AC common-mode voltage	-150	-	150	mV pkpk
T RX-DDJ	Receive input signal data dependent Jitter (Inter-symbol interference)	-	-	1	UI pkpk

T RX-RJ	Receive input random jitter	-	-	0.3	UI pkpk
T RX-PJ	Receive input period jitter (At high frequency)	-	-	0.1	UI pkpk
T RX-TJ	Receive input Total Jitter (DDJ + RJ + PJ).	-	-	1	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-pass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to the data rate	-	1667	-	F BAUD /F GPLL

Receive Loop Loss Table 10

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Receiver differential DC return loss	-	-	**-20**	dB
Z RL-DIFF-NYQ	Receiver differential return loss at 5.0 GHz	-	-	-2.5	dB
Z RL-CM-DC	Receiver common-mode DC return loss	-	-	-10	dB
Z RL-CM-NYQ	Receiver common-mode return loss at 5.0 GHz	-	-	-5	dB

Receive DC Resistance Table 11

Parameter	Description	Min.	Typ.	Max.	Units
R DIFF-DC	DC differential receive impedance	80	100	**110**	Ω
R CM-DC	DC common-mode receive impedance	20	25	**27.5**	Ω
R DIFF-HIZ-POS	Differential receive high-impedance for input voltage from 0 V to 200 mV	200k	-	**-**	Ω
R CM-HIZ-POS	Common-mode receive high-impedance for input voltage from 0 V to 200 mV	20k	-	**-**	Ω
R DIFF-HIZ-NEG	Differential receive high-impedance for input voltage from -150 mV to 0 mV	4k	-	**-**	Ω
R CM-HIZ-NEG	Common-mode receive high-impedance for input voltage from -150 mV to 0 mV	1k	-	**-**	Ω

Received Signal Detection Table 12

Parameter	Description	Min.	Typ.	Max.	Units
V IDLE-THRESH	Receiver signal detect input voltage threshold	75	120	**175**	mV diff-pkpk
T SIGDET-ATTACK	Signal detect valid signal attack time (Turn-on time) in SATA mode	-	-	**15**	ns
T SIGDET-DECAY	Signal detect valid signal decay time (Turn-off time) in SATA mode	-	-	**15**	ns

T SIGDET-ATT-DECAYMIS	Signal detect attack/decay time mismatch in SATA mode	-	-	**5**	ns

4.5.2 Transmit Direction Parameters

Output Eye Diagram Characteristics Table 13

Parameter	Description	Min.	Typ.	Max.	Units
V TX-DIFF-PKPK	Backporch transmit amplitude	400	-	**1400**	mV diff-pkpk
V TX-EYE-PKPK	Transmit eye voltage opening	400	-	**1200**	mV diff-pkpk
D TX-N+1-DEEMP	N+1 precursor tap De-emphasis	0	-	**5.0**	dB
D TX-N-1-DEEMP	N-1 postcursor tap De-emphasis	0	-	**8.5**	dB
D TX-N-2-DEEMP	N-2 postcursor tap De-emphasis	0	-	**2.0**	dB
T TX-SLEW	Rise/Fall time	30	-	**120**	ps
T TX-PJ	Transmit periodic jitter Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	**0.05**	UI pkpk
T TX-RJ	Transmit total peak-to-peak random jitter (Assumes 14 TXRJ-RMS) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	**0.15**	UI pkpk
T TX-TJ	Transmit total peak-to-peak jitter (Assumes T TX - TJ = T TX-DDJ + T TX-PJ + T TX-RJ) Assumes a 1 st order high-pass jitter measurement filter with a cutoff of F BAUD /F GPLL = N GPLL	-	-	**0.25**	UI pkpk
N GPLL	F 3dB cutoff frequency for 1 st order high-sass jitter measurement filter Defined as the ratio of the F 3dB cutoff frequency, to the data rate	-	1667	**-**	F BAUD / F GPLL
V TX-CM-PKPK-AC	AC common-mode voltage	-	-	**100**	mV

	variation (Peak-to-peak) at PCIe Gen2 rate				
V TX-CM-RMS-AC	AC common-mode voltage variation (RMS) at PCIe Gen1 rate	-	-	**20**	mV

Send DC Characteristics Table 14

Parameter	Description	Min.	Typ.	Max.	Units
Z TX-DIFF-DC	Transmitter output differential DC impedance	80	100	**120**	Ω
Z TX-CM-DC	Transmitter output common-mode DC impedance	20	25	**30**	Ω
Z TX-DIFF-HIZ	Transmitter output differential DC impedance in squelch mode	-	-	**>2k**	Ω
Z TX-CM-HIZ	Transmitter output common-mode DC impedance in squelch mode	-	-	**> 500**	Ω

Send Loop Loss Table 15

Parameter	Description	Min.	Typ.	Max.	Units
Z RL-DIFF-DC	Transmitter differential DC return loss	-	-	**-20**	dB
Z RL-DIFF-NYQ	Transmitter differential return loss at 5.0 GHz	-	-	**-4**	dB
Z RL-CM-DC	Transmitter common-mode DC return loss	-	-	**-10**	dB
Z RL-CM-NYQ	Transmitter common-mode return loss at 5.0 GHz	-	-	**-5**	dB

Idle Condition Table 16

Parameter	Description	Min.	Typ.	Max.	Units
V TX-IDLE	Idle output voltage	-	-	**20**	mV pkpk
V CM-DELTA-SQUELCH	Maximum common-mode step entering/exiting squelch mode	-	-	**50**	mV
T TX-IDLE-LATENCY	Latency entering/exiting idle	-	-	**8**	ns

Receive Detection Table 17

Parameter	Description	Min.	Typ.	Max.	Units
V TX-RCV-DETECT	Voltage change allowed during receiver detection	-	-	**600**	mV

4.6 GEPHY Interface Parameters

DC Electrical Characteristics Table 18

Parameter	Description	Min.	Typ.	Max.	Units
VIH	Input High Voltage	2	-	3.465	V
VIL	Input Low Voltage	-0.3	-	0.8	V
VOH	Output High Voltage	2.4	-	-	V
VOL	Output Low Voltage	-	-	0.4	V
IOH	High Level OutputCurrent @V OH,min	-	9.3~41.8	-	mA
IOL	Low Level Output Current @V OL,max	-	6.3~27.7	-	mA

AC Electrical Characteristics Table 19

Parameter	Symbol	Description	Min.	Typ.	Max.	Units
Receiver Electrical Characteristics						
Input Voltage	Vid	AC coupled, differential p-p	50	–	1000	mV
Signal Detection	Videct	Differential peak	–	40	–	mV
Input impedance	Rin,100	Differential on-chip	80	100	120	Ω
Transmitter Electrical Characteristics						
Output when DISABLED	–	–	–	–	30	mV
Output impedance	Rout,100	Differential On-chip	80	100	120	Ω
Output amplitude	Vodpp	Differential p-p	400	–	1200	mV
Common Mode Output Level	Vocm	–	–	500	–	mV

5 Crystal Input

The 5VT2510 run off a single 25MHz,fundamental mode crystal,could use crystal or oscillator,crystal specification as following:

Table 20

Symbol	Meaning	Min.	Typ.	Max.	Units
VIH	Input high voltage	2.0	--	--	V
VIL	Input low voltage			0.8	V
Tfrequency	Clock frequency		25		MHz
Δ frequency	Clock tolerance	-50	-	50	ppm
C1	Load cap	12		27	pF
C2	Load cap	12		27	pF
Tdc	Duty cycle		50%		%

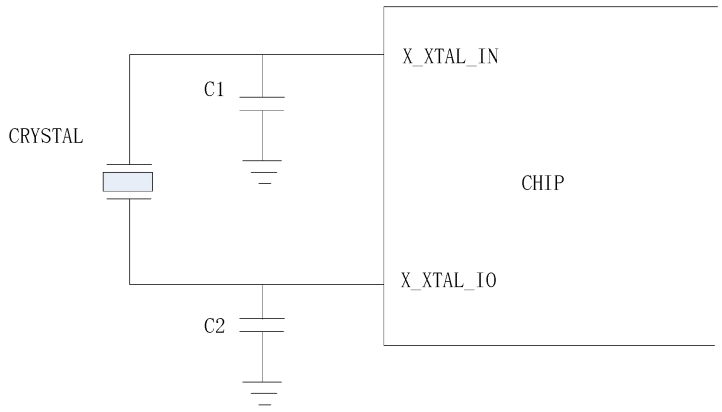


Figure 8 Crystal Circuit Diagram

6 Reliability Characteristics

6.1 Reliability Parameters

Table 21

Reliability Parameter	Max.	Units	Remark
HBM	2K	V	

CDM	500	V	
MM	200	V	
Latch-up	200	mA	
MSL	3	级	

6.2 Maximum Working Environment

Table 22

Parameter	Symbol	Min.	Max.	Units
Junction temperature limit	Tj	-40	+125	℃

6.3 Recommended Working Environment

Table 23

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambient temperature	Ta	-20	25	85	℃
Welding temperature	Tp	225	235	245	℃
Junction temperature	Tj	-40	-	125	℃
Storage humidity	Ts	-55	-	150	℃
Relative humidity	RH	-	50	90	%

6.4 Thermal Characteristics

Thermal Resistance Table 24

Theta Ja (˚C/W)			Psi jt (˚C/W)	Theta Jc (˚C/W)	Theta Jb (˚C/W)
0 m/s	1 m/s	2 m/s			
29	23.7	22.5	0.27	9.5	12.38

7 Power Parameters

7.1 Power Dissipation

Maximum power dissipation: 1.4W

Typical power dissipation: 1W

Standby power dissipation：0.7W

7.2 Maximum Supply Current of Each Branch

Table 25

Power Pin's Name	**Number**	Voltage(V)	Voltage range	Ripple Requirements	Maximum power supply requirement (mA)	Power Supply
VCC33A_GPHY	2	3.3	±10%	30	96.7	Analog power 3.3V
VCC2IO_VDD	2	2.5	±8%	NA	50	KGD 2.5V power
VCCK	12	1.1	-5%~+10%	NA	300	Digital power 1.1V
VCC2IO_CMD	1	2.5	±8%	NA	49	DDR 2.5V power
VCC2IO_BYTE0	2	2.5	±8%	NA		DDR 2.5V power
VCC3A_OSC	1	3.3	±10%	NA	2.5	Analog power 3.3V
VCC25A_SC_PLL	1	2.5	±10%	10mV	4.4	Analog power 2.5V
VCC11P_SC_PLL	1	1.1	-5%~+10%	10mV	1.5	Analog power 1.1V
VCC25A_GEPON	2	2.5	±10%	Below 30mV@10Mhz Above	34	Analog power 2.5V

				50mV@10Mhz		
VCC11A_GEPON	2	1.1	-5%~+10%	Below 30mV@10Mhz Above 50mV@10Mhz	48	Analog power 1.1V
VCC11A_SYS_PLL	1	1.1	-5%~+10%	35mV	5	Analog power 1.1V
VCC11A_DDR_PLL	1	1.1	-5%~+10%	35mV	5.5	Analog power 1.1V
VCC3IO_1	3	3.3	±10%	Digital power processing	70	DigitalIO3.3V
VCC11A_DLL_BYTE0	1	1.1	-5%~+10%	35mV	20	Analog power 1.1V
VCC3IO_2	3	3.3	±10%	Digital power processing	40	DigitalIO3.3V
VCC11A_GPHY	1	1.1	-5%~+10%	15	113	Analog power 1.1V

7.3 Power-Up Sequence

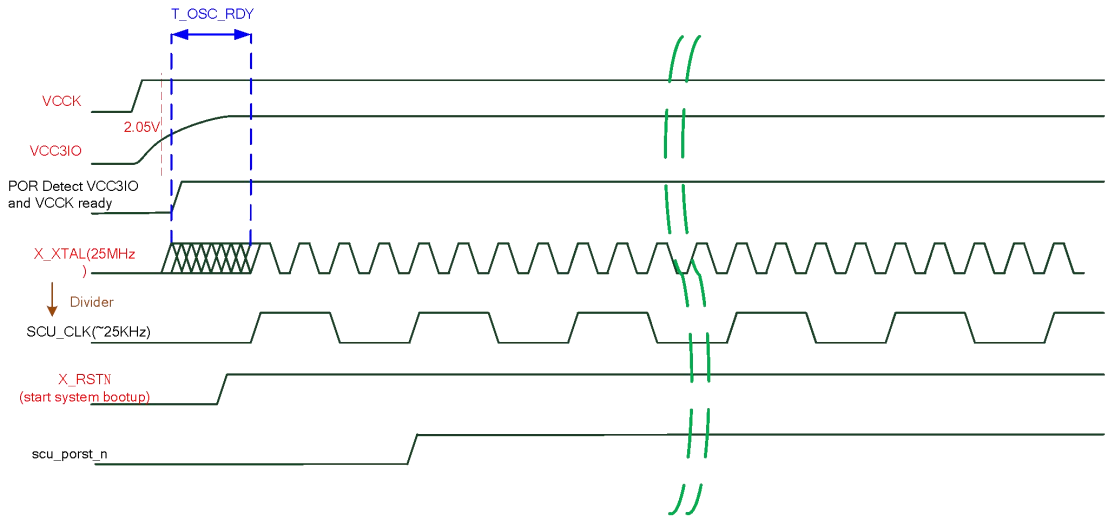


Figure 9 Chip Power-on Sequence Diagram

Notice:

1. VCC3IO should be powered on after the VCCK;
2. The built-in counter in POR starts counting 200ms (T_OSC_RDY) after the crystal clock vibrates. It is required that the crystal stabilization time must be less than 200ms;
3. The minimum voltage at which POR triggers its reset release is 2.05V;
4. The reset of POR output is released after 200ms, POR output will be reset as the starting

point if X_RSTN is released within 200ms, while X_RSTN reset release as the starting point if its reset is released after 200ms;

5. SCU_ CLK is obtained through the frequency division of a 25MHz crystal clock.

Table 26

Symbol	Description	Maximum Value	Units
T_OSC_RDY	Crystal power-on stabilization time	200	ms

8 Mechanical Characteristics

Packaging Characteristics

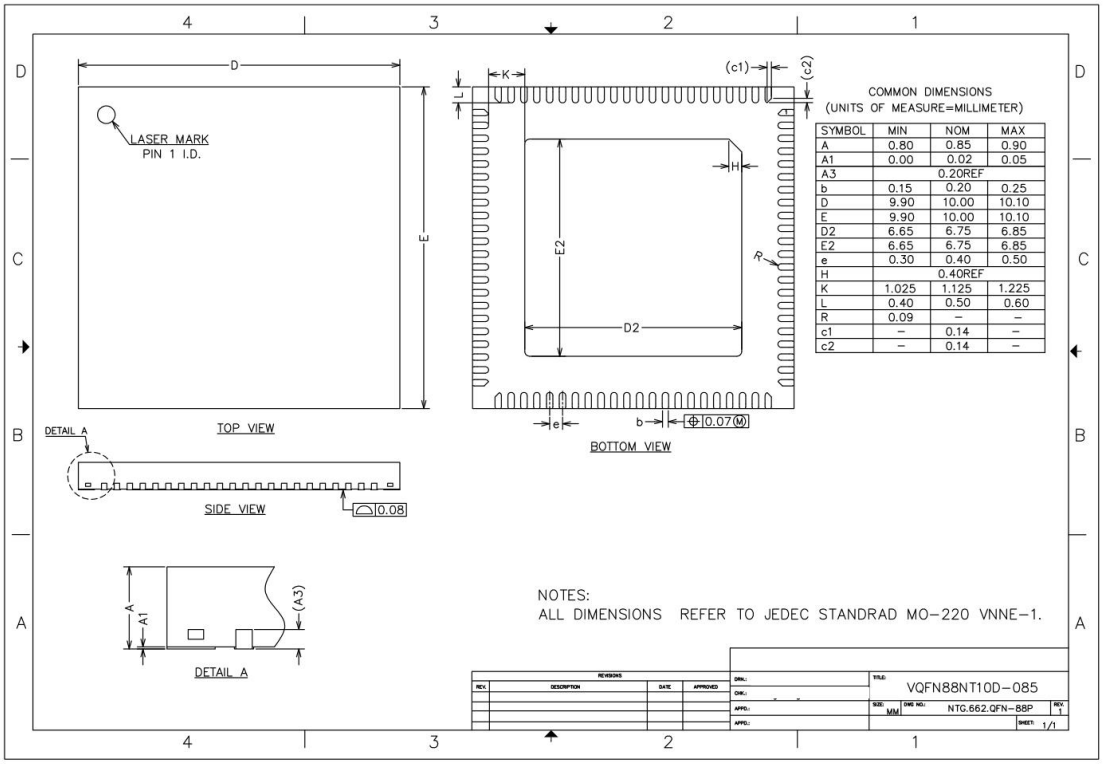
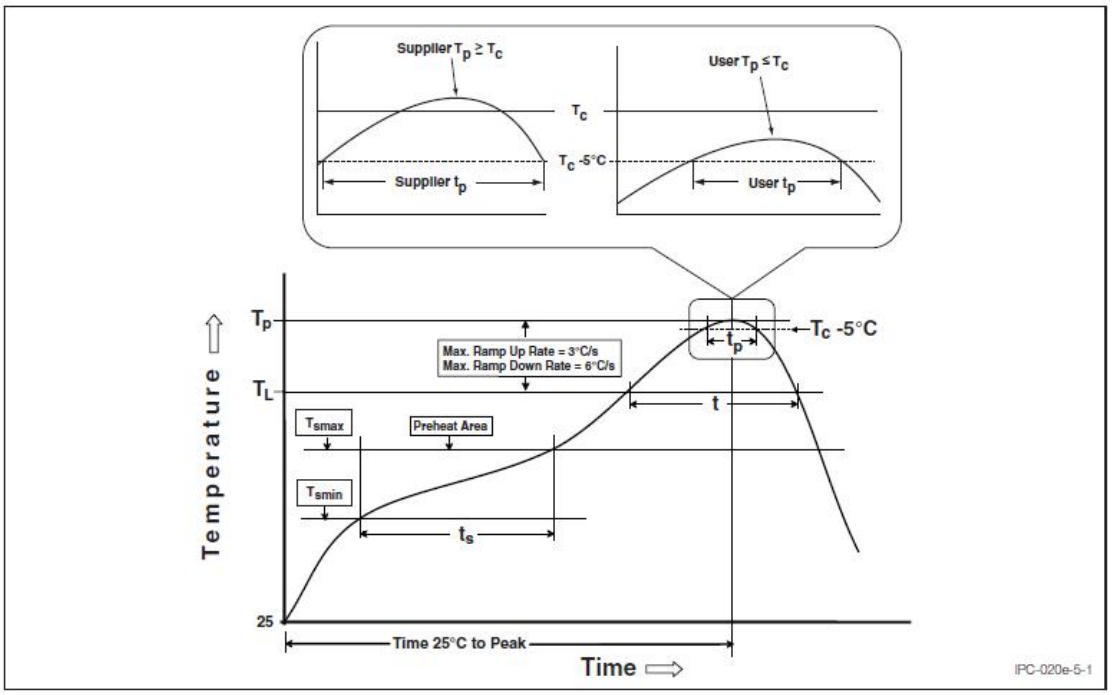


Figure 10 Packaging Physical Dimensions

9 Reflow Profile



Profile	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat and soak Min. temperature (Ts_{min}) Max. temperature (Ts_{max}) Time (ts_{min} to ts_{max}) (t_s)	 100 °C 150 °C 60 ~ 120 seconds	 150 °C 200 °C 60 ~ 120 seconds
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second (Max.)	3 °C/second (Max.)
Liquid temperature (T_L) Time at liquid (t_L)	183 °C 60 ~ 150 seconds	217 °C 60 ~ 150 seconds
Peak package body temperature (T_p)*	235℃	260℃
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to Ts_{max})	6 °C/second (Max.)	6 °C/second (Max.)
Time to peak temperature from 25 °C	6 minutes (Max.)	8 minutes (Max.)
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		