5VT 5VT6126

Datasheet

Issue R2.0

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1 About This Document

1.1 Purpose and Audience

This document describes the functionality, interfaces, signals, physical requirements, and the operating environment of 5VT6126. It is intended for hardware, software, and application developers who need to understand 5VT6126.

1.2 Acronyms and Abbreviations

Table 1-1 : Acronyms and Abbreviations

Acronym	Definition
ACL	Access Control List
AFT	Accept Frame Type
APS	Automatic Protection Switching
CFlex LAG	5VT Flexible Link Aggregation
DDR	Double Data Rate
DRR	Deficit Round Robin
DVMRP	Distance Vector Multicast Routing Protocol
ECMP	Equal-Cost Multi-Path
GE	Gigabit Ethernet
GRE	Generic Routing Encapsulation
IGMP	Internet Group Management Protocol
ISATAP	Intra-Site Automatic Tunnel Addressing Protocol
IVI	IPv4-derived IPv6
IVL	Independent VLAN Learning
LPM	Longest Prefix Matching
LSP	Label Switch Path
MAC	Media Access Control
MDC	Management Data Clock
MDIO	Management Data Input/output
MSTP	Multiple STP
NAPT	Network Address Port Translation

Acronym	Definition
NAT	Network Address Translation
NAT-PT	Network Address Translation-Protocol Translation
NVGRE	Network Virtualization using Generic Routing Encapsulation
OAM	Operation Administration Management
PBR	Policy Based Route
PBT	Provider Backbone Transport
PHP	Penultimate Hop Popping
RPF	Reverse Path Forwarding
RSPAN	Remote Switched Port Analyzer
RSTP	Rapid STP
SIIT	Stateless IP/ICMP Translation
SP	Strict Priority
STP	Spanning Tree Protocol
SVL	Shared VLAN Learning
TCAM	Ternary Content-addressable Memory
VC	Virtual Connection
VFI	Virtual Forwarding Instance
VPLS	Virtual Private LAN Service
VPWS	Virtual Private Wire Service
VRF	Virtual Route Forwarding
VXLAN	Overlaying Virtualized Layer 2 Networks over Layer 3 Networks
WRR	Weighted Round Robin
XAUI	10 Gbps Attachment Unit Interface
DXAUI	20 Gbps Attachment Unit Interface
XLAUI	40 Gbps Attachment Unit Interface
QSPI	Quad Serial Peripheral Interface
SPI	Serial Peripheral Interface

1.3 Reference

Table 1-2 : Reference Documentation

Documents Name	Description
5VT6126 Advanced Hardware design guide	Advanced hardware design info with 5VT6126

1.4 Revision History

Date	Version	Description	Page
2020-07-08	R1.10	Add note “NOTE： All interfaces need to be configured for normal operation. ” for section 6.1	39
		Add working condition for Endpoint mode that 5VT6126 needs to release reset(RST_SUP_B) 5ms earlier than external CPU.	47
		Add “It is recommended that 5VT6126 and external CPU use the same origin clock.” for PCIe interface	47
		Update Boot_usb_vreg_byp description in table 8-1 to: 0： MSH internal logic uses clock generated from MSH_CLK 1: MSH internal logic uses internal clock. It is recommended to implement compatible design, and the default is pull-down.	94
		Delete Note3 for table 9-2	105
		Update the QSPI_CLK rate to 25MHz in table 8-1	90
		Update pin USB_VBUS0 description in table 8-1 to “OTG function not supported. Leave this pin floating”	93
		Modify some typos and misspellings	
2020-04-28	R1.9	Update Marking info in section 12.2	122
		Add operating Ta specification in table 9-2, update the Note[2] of table 9-2	100
		Delete the minimum rating of Tj in table 9-1, and add caution description for table 9-1	99
		Add note[7] for table 8-1, and delete the “PD/PU” indication of output only pin.	87, 94, 95, 96
		Update ESD reference standard in table 9-1	99
		Update the diagram of Sync Ethernet Clock Scheme	48
2020-02-28	R1.8	Delete DDR4-1866 spec in table 10-16	115
		Delete support SPB	15
		Delete support SD in Ethernet OAM	25
2020-01-22		Update the description of ‘DDR_CS_B[3:0]’ in table 8-1	89
2019-12-19	R1.7	Delete description about ‘High Speed DDR’ of eMMC, update the DDR_CLK frequency of DDR4 from 1200MHz to 800MHz in table 8-1	90, 115, 116
		Delete support of SD card, and update the description about SD_DET_B/ SD_WP/ SD_SW_VOLT_EN in table 8-1	19, 38, 45, 88,89,90, 96,104, 115,116
		Delete the Note ‘The clock Signals Sequence #1~#5 should come from same clock source’ about table 10-1	108
		Update the Note[5] description in section 8.1	85

Date	Version	Description	Page
		Update the DDR4/DDR3 Timing parameters in table10-16,table10-17	117,118
2019-10-23		Add the capability about Macsec and Cloudsec	14
		Update the frequency ofCS_REFCLK_P/ CS_REFCLK_N to156.25MHz in table6-1	39
2019-09-24	R1.6	Update the description of HSS_REFCLK_P/ N in table 8-1	86
		Update the description of HSS_REFCLK_P/N in table 10-1	107
2019-07-26	R1.5	Update the Clock signal requirements in table 10-1 and update the description of Note3	107
		Update the maximum value of V_{IH} to 3.6V in table 9-8, table 9-10	103
2019-07-08		Update the Clock signal requirements in table 10-1	107
		Update the description about Tcss and tCSH	113
		Update the SPI Interface Timing Diagram of figure 10-8	113
		Update the default state of pin BOOT_PCIE_FORCE_MODE from 'PD' to 'PU' in table 8-1	86
		Update the description of MSDA[0:1] in table 8-1	93
2019-06-12	R1.4	Update the description about VDDIO18_EFUSE_INFO and VDDIO18_EFUSE_MEM in table 8-2	96
2019-05-22	Preliminary R1.3	Update the minimum value of fCK and the maximum value of tCK in table 10-12 and table 10-13	113, 114
2019-05-17		Update the description about SMI interface operation	48
		Add note[6] for pin information	83
		Update the description of note[3] in table 10-1	106
2019-05-05		Delete the description about 'Energy Efficient Ethernet'	18, 33, 41
		Update the unit of tr and tf in table 10-6	109
2019-04-23		Update the description about BOOT_RESV	87
2019-04-12		Update eMMC interface timing parameter '3.0V' to '3.3V' in section 10.11	115
		Add Reflow profile in figure 11-1	120
2019-04-10		Update the power Requirements for different voltage in table 9-7	102
2019-04-04		Update the maximum tSLEW value in table 9-4	100
		Update the power consumption in table 9-5,9-6	101
2019-03-18	Preliminary R1.2	Delete the description of "CKE[3:2] used for twi-die application" about DDR_CKE[3:0]	89
		Delete the description of "ODT[3:2] used for twi-die application" about DDR_ODT[3:0].	90
2019-03-12		Update the description of PN swap	33
		Delete the support of 50GAUI2	38, 39, 85

Date	Version	Description	Page
2018-12-28	Preliminary R1.1	Update the description about DDR_CS_B[3:0]	
2018-12-19		Update power on sequence	
2018-12-10		Fix bug	
2018-12-03		Update DDR_VREF/MSH_RST_B/ parameters	
2018-09-21	Preliminary R1.0	First release	

2 5VT6126 Introduction

The 5VT®5VT6126 is a purpose built device to address the challenge in the recent Network evolution such as Cloud computing.To offer enhanced system function integration with lower system BoM cost, the 5VT6126 family combines a feature-rich switch core and an embedded ARM A53 CPU Core running at 800MHz/1.2GHz. 5VT6126 provides 440G I/O bandwidth and 400G core bandwidth. It equips 24 of 13G SerDes Lanes and 8 of 28G SerDes Lanes. As a highly integrated chip, 5VT6126 is an ideal choice for edge switch design in Cloud Era with form factors like 32x 10GE or 48x1GE/2.5GE + 4x25G +2x50G.

As the 6th generation of 5VT TransWarp™ family, 5VT6126 is built on the field proven 5VT switch architecture to provide Layer2, Layer3, MPLS, and VXLAN features. In addition, leveraging the internal IPFIX Engine, 5VT6126 supports the statistics of session-based service, packet-drop, and the water mark of latency and jitter. 5VT6126 offers the advanced features such as ASE256-based MACSec and CloudSec capability, Segment Routing up to 10 level MPLS Labels, IEEE1588v2, etc. Meanwhile, the pipeline of 5VT6126 is optimized for XGPON application in 5G network. 5VT6126 supports flexible programmability for tunneling process which identifies the unknown Layer2, Layer3 and Layer4 tunnel. Furthermore, it supports to en-capsulate, de-capsulate, and edit these unknown tunnels so it is able to provide the wire-speed solution for PPPoE, GTP, and G.INT tunnel application.

The key features as supported by 5VT6126 are listed below:

- 9MB embedded packet/table shared buffer with self-tuning threshold for more evenly and efficient bufferusage
- On-chip CAPWAP engine for wireless application such as CAPWAP De-capsulation/ Encapsulation, CAPWAP Fragment/ Reassembly and hardware-based solution for CAPWAP Roaming
- On-chip Flow Tracing Engine for advanced NetFlow sampling(IPFIX)
- Centralized Security-Engine™ technology with advanced security features to provide high performance networking security such as MACSec (IEEE 802.1AE and IEEE 802.1AX) and CloudSec (VXLAN Based Encryption and Decryption) with 100G Encryption and 100G Decryption capability. More details can be found in Programming Guide
- CoPP (Control Plane Policing) for CPU traffic protection
- On-chip OAM engine supporting Ethernet OAM/ BFD/ MPLS-TPOAM
- Embedded traffic manager providing 12 basic queues per port and 3K extra service queues which can be assigned to each port flexibly to meet the application requirement.
- Support NVGRE andVXLAN
- Support Data Center Features including PFC, ETC, VEPA, TRILL, FCoE,etc.
- Cut-Through forwarding for lower and fixed latency.

- Rich monitoring and diagnostic features for trouble shooting
- Large flow table for SDN/OpenFlow
- IPv4/IPv6 dual-stack forwarding with translation technologies
- Support Jumbo Frame up to 9600 Bytes

3 Device Overview

3.1 Packet Process Pipeline

5VT6126 follows the same truly distributed and service-aware architecture of 5VT TransWarp™ Family to provide:

- Truly distributed ingress/egress packet processing for both unicast andmulticast
- Scalable for both pizza-box and central forwarding system with dynamic port configuration

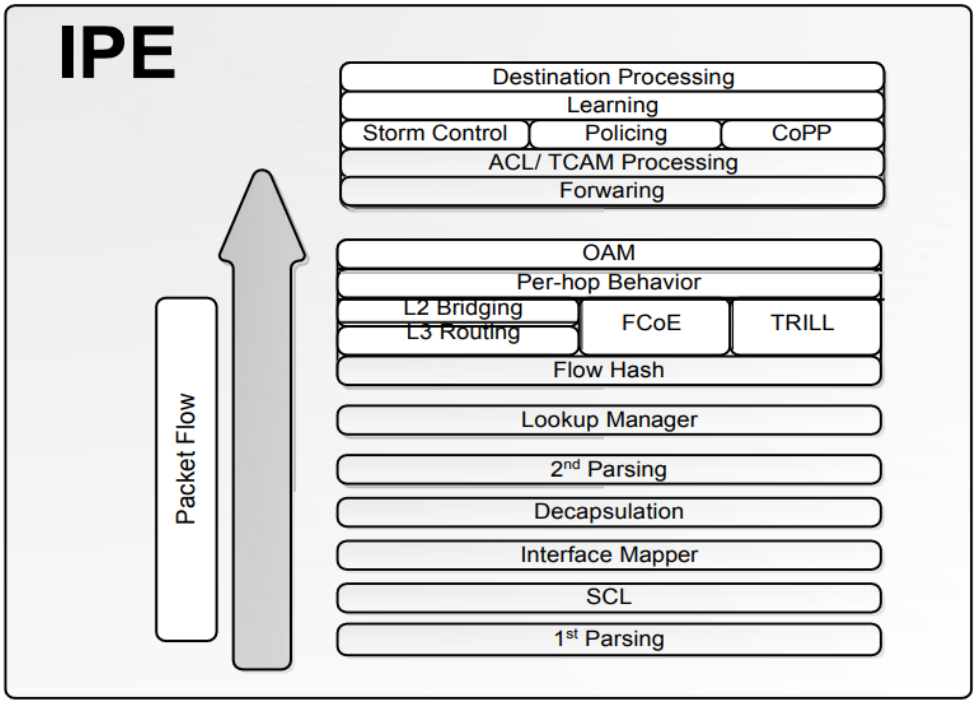

Figure 3-1 : The IPE (Ingress Packet Engine) pipeline in 5VT6126

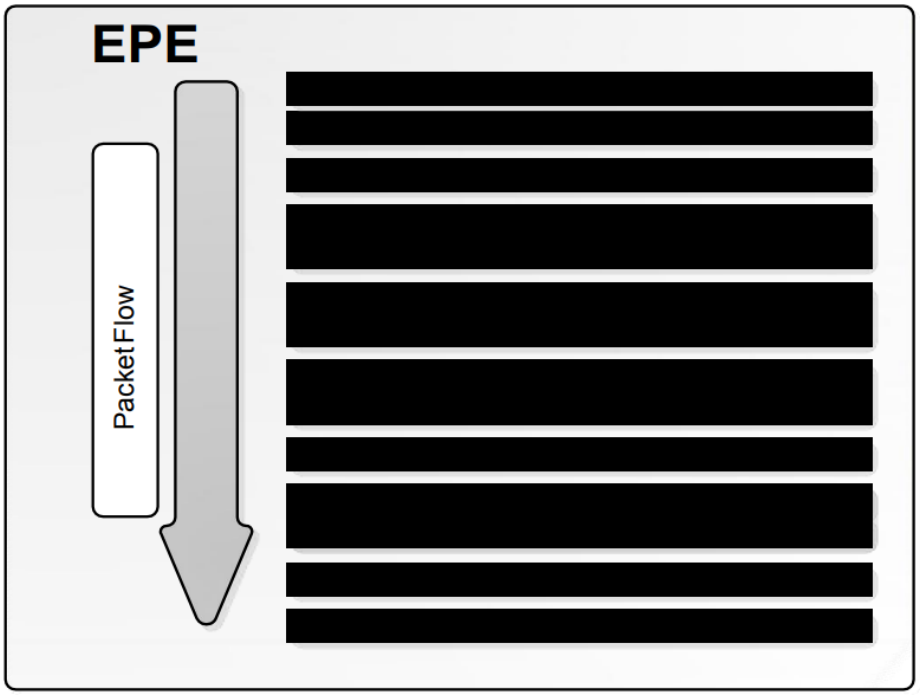

Figure 3-2 : The EPE (Egress Packet Engine) pipeline in 5VT6126

3.2 Core and I/O Bandwidth

3.2.1 400G Core Bandwidth

5VT6126 delivers 400Gbps line rate performance for all packet-length except for 145bytes and 146 bytes. At 400G bandwidth, all ports can meet the requirement of the RFC2544 test.

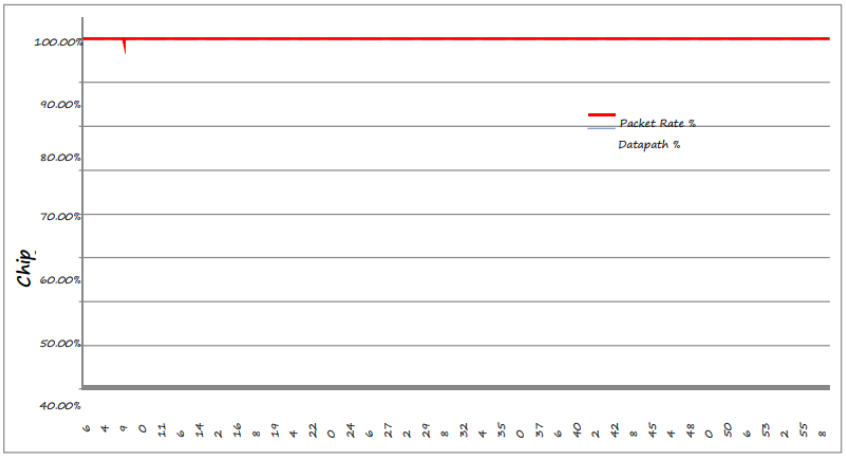

Figure 3-3 : Chip performance for 400Gbps bandwidth

3.2.2 440G I/O Bandwidth

5VT6126 supports 440G I/O bandwidth. The Typical form factor is 24 x 10G + 2 x 100G. It supports over subscription to maximize I/O throughput. For example, user can configure one 100G port as the highest forwarding priority without packet loss.

Table 3-1 : Packet Size of Oversubscription with different bandwidth

Bandwidth	Packet Size of Oversubscription
440G	64B~71B，145B~163B
400G	145B~146B

3.3 Feature List

Table 3-2 : 5VT6126 Features List

Feature	Description
Octal SerDes Macro	Three HSS Macros provide up to 24 SerDes Lanes. Flexible SerDes configuration to operate in any of the following port mode (For more details, please refer to *5VT6126_ Port_Application_Note*): • 40GbE (4-lane) KR4/ CR4/ SR4/ ER4/ LR4/ with Base-R FEC (FC(2112,2080)) • 10GbE (1 lane) XFI/ SFI/ KR/ CR/ SR/ ER/ LR/ with Base-R FEC (FC(2112,2080)) • 10GbE (4-lane)XAUI • 5GbE (1-lane) QSGMII (Only 12 of QSGMII PCS interfaces are supported) • 2.5GbE 2500 BASE-X (1-lane) • 1GbE (1 lane) SGMII with 10M/100M/ 1000M SGMII AN, IEEE802.3 clause 37AN • 1000 BASE-X (1-lane) with 1000M IEEE802.3 clause 37AN • 100M (1-lane) 100BASE-FX interface • 10G USXGMII-M Multiple Mode: 2 of 10M/100M/1G/2.5G/5G ports or 4 of 10M/ 100M/ 1G/2.5G/ mode(Only support 12 of USXGMII PCS interfaces

Quad SerDes Macro	8 high speed SerDes lanes to provide 1.25G~28.125G lane speed with the following standards: • 100GbE (4-lane) KR4/ CR4/ SR4/ ER4/ LR4/CAUI4 • 50GbE (2-lane), support RS-FEC and Base-RFEC • 40GbE (4-lane) KR4/ CR4/ SR4/ ER4/ LR4/ • 25GbE (1-lane), support RS-FEC and Base-RFEC • 10GbE (1-lane)XFI/SFI/KR/CR/SR/ER/LR • 10GbE (4-lane)XAUI • 1GbE (1 lane) SGMII with 10M/100M/ 1000M SGMII AN, IEEE802.3 clause 37AN • 1000 BASE-X (1-lane)with 1000M IEEE802.3 clause 37AN
Interface	100M/1G/2.5G/5G/10G/20G/25G/40G/50G/100Gbps speed, configured or auto-negotiated

Feature	Description
	Standard MAC MIB
	Optional network port act as dedicated CPU traffic port
	x1 PCIe 2.0 for External CPU configuration and traffic interface
	OoBFC
	CPU burst I/O access mode
	MDIO 1G/10G read/write/scan
	MAC LED
	I^2C Master Interface
	I^2C Slave Interface
CPU Interface	• 2 of SGMII interfaces • GPIO Interface • DDR3/4 Interface • QSPI interface • SPI Interface • MDIO Interface • USB2.0 Interface • PCIe Gen1/Gen2 • 3 of UART Interfaces • eMMC Interface • 2 of I^2C Soc Interface
L2 Bridging	SVL and IVL
	Hardware-based MAC learning and aging
	Station movement control
	Fast MAC flush per port/VLAN/port + VLAN
	Per VLAN / destination port controlled unknown discard for unicast /multicast / broadcast
	Unknown unicast/multicast/broadcast to CPU
	Static MAC
	Per port L2 protocol packet processing
	Port random log
	Access/trunk/hybrid port support
	Flexible AFT (per port accept/deny packets according to any combination of C-TAG and S-TAG)
	SW MAC learning and aging
	Black Hole MAC
	White List
	Dump MAC by port/ vlan / port+ vlan /MAC/MAC-fid
	Dump MAC by dynamic /static/all
	Dump MAC sort by trie tree
	Logic port learning for L2VPN

Feature	Description
VLAN	Support C-VLAN and S-VLAN
	Global C-VLAN TPID and S-VLAN TPID setting and per port S-VLAN TPID selection
	Ingress and egress VLAN filtering
	Single or double tags VLAN translation on both ingress and egress
	Any combination of adding/replacing/removing operation for CVID /C-TAG CoS / C-TAG CFI / SVID / S-TAG CoS / S-TAG CFI on both ingress and egress
	VLAN classification based on MAC SA/MAC DA/IP SA/IP DA/any L2 fields combination/protocol/port
	Single or double tag VLAN switching
	Private VLAN
	VLAN RX / TX statistics
	Spanning Tree，MSTP, RSTP
L2 Multicast	Per VLAN IGMP packet processing
	L2 multicast to physical port or tunnel
	PIM snooping
	Discard or send to CPU for unknown multicast packets
	IPDA, MACDA two level lookup
	IP base l2 multicast
Storm Control	Per port / VLAN storm control
	Both bits per second and packets per second rate limit
	Support unknown unicast /unknown multicast/ broadcast/ known unicast /known multicast /all unicast /all multicast rate limit
	Per MAC address rate limit
	Per port per packet type configurable threshold
Port LAG	Route Selection： • Static load balance forLAG • Regular and Random round-robin for LAG • Flowlet-based dynamic load balance forLAG • Resilient hashing forLAG • Forwarding mode for local members with higher priority
	Fault Tolerance： • Hardware-based LAG failover mechanism
Channel or CFlex LAG	Route Selection： • Static load balance forLAG • Regular and Random round-robin for LAG • Flowlet-based dynamic load balance forLAG • Resilient hashing forLAG
	Fault Tolerance： • Hardware-based LAG failover mechanism
ECMP	Route Selection：

Feature	Description
	• Static load balance forECMP • Regular and Random round-robin for ECMP • Dynamic load balance forECMP • Resilient hashing forECMP
	Fault Tolerance： • Hardware-based ECMP failover mechanism • Self-Healing for ECMP
HASH mechanism	Fields for HASH: • L2: MAC SA / MAC DA / SVID / CVID / S-TAG CoS / C-TAG CoS/EtherType • L3: IP DA/IP SA/IP header protocol/MPLSlabel • L4: TCP src/dest port, UDP src/dest port • Tunnel: Inner header's fields/outer header'sfields/Inner+outer • Based on entropy information, for example: VXLAN, NVGRE, MPLS with entropy label
	Symmetric hashing
L3 Routing	4K Layer 3 interface, including VLAN interface and routed port
	Per L3 interface L3 protocol packet processing
	Per VLAN DHCP/ARP handling
	IPv4 and IPv6 host route
	Algorithm based IPv4 and IPv6 LPM (TCAM-based lookup is also supported)
	Public and Private route
	ECMP
	Loose and strict RPF check
	VRRP
	ICMP redirect check
	Virtual Route Forwarding, up to 8K instances
IP Tunneling	Static V4inV4, V6inV4, V4inV6, V6inV6 tunnel
	6to4 tunnel
	ISATAP tunnel
	GRE tunnel with Ethernet/IPv4/IPv6/MPLS/User Defined Type as payload
	UDP tunnel uRPF
IP Overlay	VXLAN / NVGRE / VXLAN-GPE / GENEVE technology
IP Multicast Routing	(S, G), (*, G), (*, *) support
	Multicast RPF check
	Physical replication (to port) and logical replication (to VLAN)
	Fallback bridge on IPMC lookup failure
	Discard or send to CPU for unknown multicast packets
	PIM Sparse and Dense mode
	Bidirectional PIM

Feature	Description
	Can be replicated to any port, VLAN, tunnel
Programmable Tunnel	Encap/ Decap and flexible editing behavior on tunnel such as PPPoE and G.INT
XGPON Pipeline	Flexible process pipeline for XGPON application
Network Security	Port/MAC based 802.1X
	Port Isolation • Per port isolation • Unidirectional and bidirectional • Isolation on flooded packets only or allpackets
	Binding with any combination of IP/ MAC/ Port/ VLAN
	DDoS Attack Prevention for: • Illegal MAC SA • Illegal IP SA • Land Attack (MAC SA==MAC DA or IP SA==IPDA) • Null scan (TCP sequence number=0, controlbits=0) • SYN/SYN-ACKflooding • Smurf attack
	Port/VLAN/System based MAC Limit
	Port Security
	CloudSec for VXLAN encapsulation
	MAC Security： • MAC Sec on everyport • MAC Sec without extra external PHY with MAC Secsupporting • Support 4 mode of MAC Security operation • ICV + encrypt all userdata • ICV + encrypt user data offset 30B fromhead • ICV + encrypt user data offset 50B fromhead • ICV only
CPU Traffic Protection	Per protocol type rate limit
	Per group rate limit (multiple protocols can be grouped)
	8 priority classes with SP/WFQ scheduling
	Total CPU traffic rate limit
	CoPP policing based on flow rules, with bps or pps
	Rate limit can be based on bps (bits per second) or pps (packet per second) unit
CAPWAP	Encap/ Decap
	Encrypt/ Decrypt (DTLS)
	Fragment/ Reassembly
	Roaming
ACL	Both ingress and egress
	Applied on port, VLAN, L3 Interface, and LogicPort

Feature	Description
	8 parallel-lookup for ingress & 3 parallel lookup for egress ACL
	Deep packet parsing up to 144 bytes
	Match all L2-L4 fields UDF
	Actions supported: • Permit/deny • Redirect to port/L3 Nexthop/multicast group/tunnel • Redirect to CPU with timestamp attached • Mirror (port, L3 Nexthop, multicast group, tunnel,CPU) • Priority and colorremark • Flow policing • Statistics • Add/remove/replace any fields in STAG and/orCTAG • Deny bridge • Deny learning • Deny routing • Random log to CPU • Select to on-chip flow tracing
	N-Flow™ technology
	Specify CPU Queue Id for traffic to CPU
	SGT • Classify based on Port, VLAN, L3Interface and LogicPort • Flexible classify based on L2-L4 fields, and FIB • Support SGT encapsulation • Support SXP (identify and redirect toCPU)
	Class group based ACL • Classify based on Port, VLAN, L3Interface and LogicPort • Flexible classify class group based on L2-L4 fields
	Policy based routing
	Forwarding Information as ACL key field
	Flexible ACL TCAM Allocation
Policing and QoS	SrTCM (RFC 2697), TrTCM (RFC 2698) and modified TrTCM (RFC 4115)
	Support both color-aware and color-blind mode
	Fine granularity down to 8K bps
	Up to 16M Bytes burst size
	256 metering/policing profiles
	MEF 10.3 BWP
	Both ingress and egress policing
	Port/ Flow/ VLAN based policing
	PPS based policing
	Aggregated policing

Feature	Description
	WRED congestion avoidance on per-queue basis, support arking for TCP traffic
	Tunnel ECN, flow-based ECN，stacking-based ECN
	CIR/PIR shaper with minimum guaranteed bandwidth and maximum regulated traffic for each queue.
	8 basic queues per port
	Each of 64 Ports has 4 NetCtl queue (2 high priorities for CPU, 2 low priorities for flooding and log/span)
	384 flexible queue groups which can be bound to ports without limitation
	8 scheduling priorities in a base queue group, SP for different priorities, WFQ for queues with the same priority.
	8 scheduling priorities in a extend queue group, SP for different priorities, WFQ for queues with the same priority.
	Configurable CIR/PIR weight, CIR is SP, PIR is SP/WFQ
	Priority propagation is from group to channel, 8 scheduling priorities in a group could be mapped to 4 scheduling priorities in a physical port
	Configurable WFQ weight between different groups
	Traffic rate regulation for all destinations by FPS (frame per second) unit
	Support packet aging and queue flush (only extend queue support)
	Ingress/Egress Resource Manage
	Flexible PHB Mapping
MPLS	Per system/per interface label space
	Full label space
	Penultimate Hop Pop
	L-LSP and E-LSP support
	Pipe/Short Pipe/Uniform Model LSP
	Parse/push/pop/lookup label number: 8/10/3/3
	Optimized Multi-Path MPLS, MPLS IP based ECMP
	Entropy label and flow label
	Martini Encapsulation
	Raw mode and tagged mode PW
	VPWS (port AC, VLAN AC)
	VPLS (port AC, VLAN AC)/H-VPLS
	L3VPN
	Multicast MPLS
	Upstream MPLS
	MPLS over GRE Tunnel
	l2/l3 Gateway
	Using TCAM resolve hash conflict
Ethernet OAM	802.1ag Connectivity Fault Management

Feature	Description
	Support both UP MEP and Down MEP
	MIP
	CCM (interval 3.3ms/10ms/100ms/1s/60s/600s)
	Link Trace (LTM/LTR)
	Loopback (LBM/LBR)
	CSF
	RDI
	APS/RAPS
	AIS
	Link OAM
	802.3ah EFM
	Y.1731 Performance Measurement
	One-way/Two-way DM
	Single-end/Dual-end LM
	QinQ OAM
	VPLS/VPWS OAM
BFD	IP BFD
	LSP BFD
	VCCV/PW BFD
	VXLAN BFD
	NVGRE BFD
	S-BFD
	Micro-BFD
	TRILL BFD
MPLS-TP OAM	Y.1731 based
	BFD based
Network Performance Management	RFC2544 for L2/L3
	Y.1564 for L2/L3
	TWAMP/OWAMP
	MEF SAT Testing (MEF46/MEF48/MEF49)
	SLM/SLR
Automatic Protection Switch	Protocol/topology independent mechanism
	One-bit flap quick switch. No need to flush forwarding table
	2-level protection switch
	Support both unicast and multicast
	Support both source and sink end
	Can be comprehensively applied to G.8031/G.8032/G.8131/G.8132/IETF EAPS/Smart Link and all other possible protection switch protocols

Feature	Description
	Hardware based APS switch
Mirror	Both ingress and egress mirror
	Port/VLAN/Flow based mirror
	32 mirror sessions
	Mirror destination: port/VLAN/tunnel/multicast group/CPU
	With extended information • Arrival timestamp • Forwarding latency • Application aware
	TCP session-sensed load balance
	Packet length truncation for log or to CPU
	Discard packet mirror • normal + discard mirror • only discardmirror
Network Time Synchronization	IEEE 1588-2008 with up to 4 management domains
	OC/BC/TC support for both 1-step and 2-step mode
	PTP over Ethernet/IPv4/IPv6/MPLS/PWE
	PTP timestamp granularity is 4ns with 250MHz reference clock
	G.8261 compliant Synchronize Ethernet with all SerDes capability
	SyncE reference selection
	Up to 3 SyncE clock output
	China Mobile ToD
	Monitor SyncE references
Data Center Bridging	Cut-Through forwarding for low latency
	PFC (Priority Flow Control) • PFC reception and stop respondingtraffic • PFC receptiontimer • Transmit PFCframe • 8 classes flow control per port
	ETS (Enhanced Transmission Selection) • 8 user configured TCs • 3 user configured TCGs • SP and DRR scheduling • BW configuration with at least 1%granularity
	Virtualization • 802.1Qbg VEPA (Virtual Ethernet Port Aggregation) • 802.1br Port Extender • Reflective relay • Port virtualization by S-VLAN on both ingress and egress • Multicast to all virtual ports • M-Tag insertion in case of multicast to portextender

Feature	Description
	TRILL • VLAN Mapping • Multi nickname per system • Multi distribution trees • Distribution tree selection based on HASH • Multi-destination frame tree adjacency check • Multi-destination frame RPF check • Multi-destination frame parallel links check • Multi-destination frame port group check • Pruning distribution treeper-VLAN • Pruning distribution tree by IGMP MLD snooping • FCoE overTRILL
	FCoE • VSAN • FCoE traffic isolated from other • FCoE access switch in switch mode • FCoE access switch in NPV mode • FPMA • SPMA • FCoE virtual link check • FCoE switching by monitoring FC header
	MLAG • MLAG Isolation
Address Translation	NAT
	NAPT
	NAT-PT
	NAT64
	IVI
CloudStacking™	Flexible topology: Ring/Tree/Line/Full mesh
	Flexible, expansible and compatible stacking Header
	Spine-leaf
	Horizontal stacking: stacking cross L2/L3 network
	Source node based load balance and loop break
	Stacking on any network port interface
TCP Sensed Flow Performance Tuning	Elephant flow detection based • Priority changing • Dynamic load balancing
	Fast packet aging for retransmitted packet
	High bandwidth ultra-low latency (HULL) policy with DCTCP
	On-chip flow tracing to support enhanced IPFIX
	Hardware IP FIX(Flow Tracing）

Feature	Description
	• Hardware Overlay Tunnel Learning • NetFlow Random Sampling and interval sampling • Hardware basedaging • New FlowExport • First N packet for new flowlog • Export based packet counter over flowor packet by teover flowor time expired or TCP session closed • Support IPFIX only when RPF Check Fail
Diagnosis	Active Buffer Monitoring
	Active Latency Monitoring
	Watermark
	Software defined counters • Off-chipstatistics • On-chip timer trigger DMA operation (DMA @) with Statistic chaining
	On-chip Packet flow path Debug Information collection
VM-Aware	Deep insight for overlay traffic to apply: • TCP sensed flow performance tuning
DMA	Packet RX/TX • User Mode and Kernel Mode • SDK in User Mode, Packet TX/RX in Kernel
	DMA Info for IPFIX/Learning/Aging/SDC/Monitor
	DMA read/write table
	DMA Sync MAC stats
	HASH Dump

3.4 Target Application

3.4.1 Enterprise Converged, 40GE/100GE uplink

5VT6126 provides two typical form factors for different enterprise applications:

- 24 x 10GE + 2x100GE(Mid-range10GE)
- 48x1G/2.5G + 4x10G + 2x40G(NBASE-T)

Highlights:

- Low power consumption and lowlatency
- Enhanced NetFlow
- SmartPort technology to support multiple port speed mode.

3.4.2 XGPON Chassis

5VT6126 is well defined for XGPON chassis application swith integrated 32Ser Desin cluding 8 of 25GE SerDes. The chip supports a typical 2: 1 convergence ratio for port bandwidth and core bandwidth in 440G-mode with sophisticated Over-sub control per port and traffic priority.It supports advanced features including VXLAN and OAM. In addition, 5VT6126 optimizes its packet processing pipeline to natively support PON service without any performance loss.

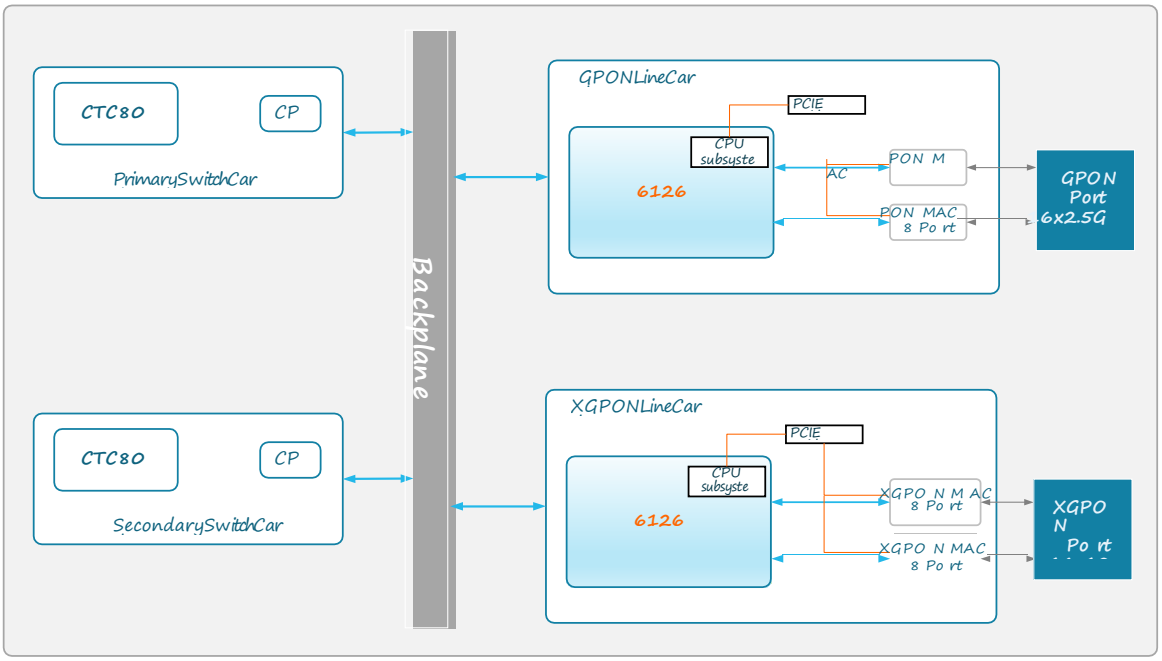

Figure 3-6 : High performance XGPON Chassis

3.4.3 G.INT Solution

Highlights for G.INT application

- Flexible Port Configuration, 1G/2.5G SGMII(UNI) and 1G/2.5G/10G/25G(NNI)
- Support TR-101Protocol
- Embedded ARM A53 Dual CoreCPU
- QinQ and Flexible QinQ, up to 3 TAGs can be processed
- SDK Ready for unique G.INT application

3.4.4 IP RANFabric

Typical Form factor: 16 x 10G + 2 x 50G + 8 x 1G

Highlights:

- Enhanced table size: LPM >128K
- Low power consumption
- Low and fixed latency

4 SmartPort™Description

4.1 Device Architecture

Figure 4-1 shows the data-path architecture of 5VT6126. 5VT6126 features 32 SerDes Lanes among of which there are two kinds of HSS Macros. One is low speed HSS Macro with Octal SerDes Lanes called Octal SerDes Macro. Each lane provides up to 12.5Gbps lane speed. The other is high speed HSS Macro with Quad SerDes Lanes, called Quad SerDes Macro. Each lane provides up to 28Gbps lane speed.

- Low speed HSSMacro
  - 3Groups
  - Speed: 1.25Gbps ~12.5Gbps
  - Each Macro: 8Lanes
- High speed HSSMacro
  - 2Groups
  - Speed: 1.25Gbps ~28Gbps
  - Each Macro: 4Lanes

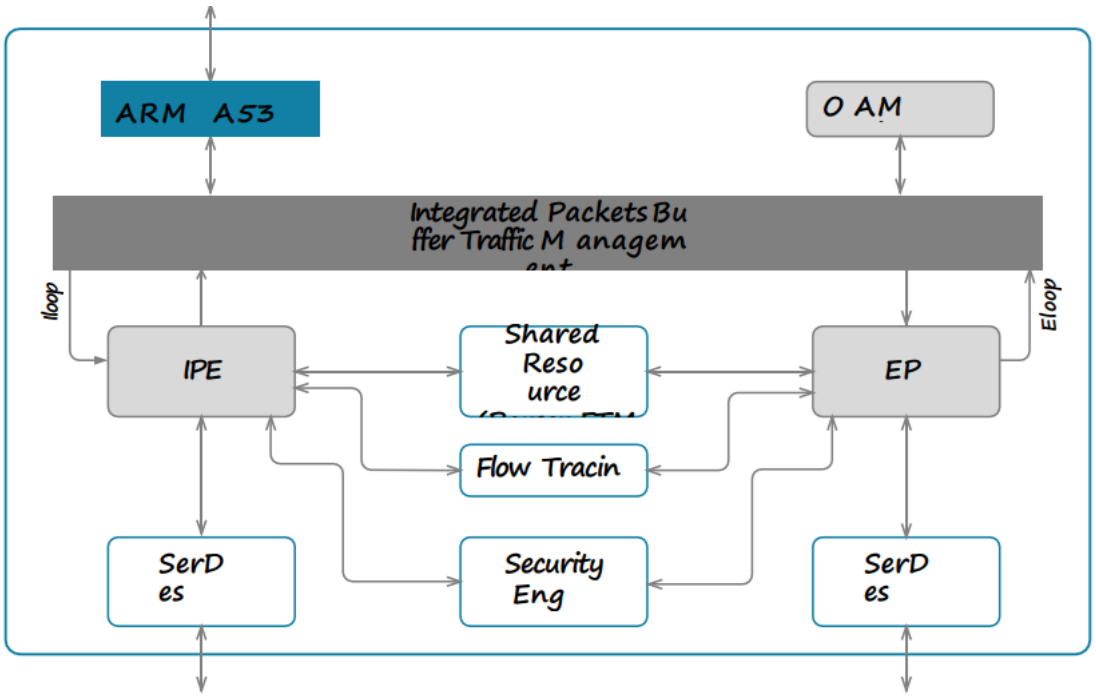

Figure 4-1 5VT6126 Data-path Architecture

4.2 SerDes Macro

Each lane in Octal SerDes Macro support PN Swap function to correct system wiring issues, which can control the polarity of both TX data and RX data. But the PN swap must be enabled/disabled at the same time on TX and RX side.

The Octal SerDes Macro in 5VT6126 is compatible with multiple industry standards including:

- 10 Gbps Ethernet application that include IEEE 802.3ak CX4 10Gb/sEthernet
- 10 Gbps Ethernet application that include IEEE 802.3ap KX KX4, and 10G-KR Ethernet over backplane
- 10 Gbps Small Form Factor Module, XFP andXFI
- Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module “SFP+”,SFF-8431
- 1Gbps Ethernet applications that include SGMII (AC-coupledonly)
- 1Gbps Ethernet applications that include IEEE 802.3z1000BASE-SX/LX
- 40 Gbps Ethernet applications that include IEEE802.3ba XLPPI, XLAUI, CR4,KR4.
- OIF-CEI-02.0 6G+ Short Reach and Long Reach and 11G+ Short Reach, Medium Reach, and Long Reach (12.5G SerDes Macro)

Each lane in Quad SerDes Macro supports PN swap function to correct system wiring issues, which can control the polarity of both TX data and RX data. The configuration of PN swap is independently between TX and RX side. Users can enable/disable PN swap on either TX data or RX data.

The Quad SerDes Macro in 5VT6126 is compatible with multiple industry standards including:

- 10 Gbps Ethernet application that include IEEE 802.3ak CX4 10Gb/s Ethernet
- 10 Gbps Ethernet application that include IEEE 802.3ap KX KX4, and 10G-KR Ethernet over backplane
- 10 Gbps Small Form Factor Module, XFP andXFI
- Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module “SFP+”,SFF-8431
- 1Gbps Ethernet applications that include SGMII (AC-coupledonly)
- 1Gbps Ethernet applications that include IEEE 802.3z1000BASE-SX/LX
- 25Gbps and 50Gbps Ethernet application
- 40 Gbps and 100Gbps Ethernet applications that include IEEE802.3ba XLPPI/CPPI, XLAUI/CAUI CR4,KR4.
- OIF-CEI-02.0 and proposed CEI-3.0 including 6G-SR,6G-LR,11G-SR,11G-LR,25G-LR,28G-SR, and 28G-VSR (28G SerDesMacro)

4.3 SmartPort™Group

5VT’s SmartPort™ architecture is designed to support dynamic port speed configuration, which enables customer to use the same silicon for different application scenarios.

In 5VT6126, there are two kinds of HSS Macros, HSS12G and HSS28G. HSS12G integrates 3 PLLs which can support 3 kinds of lane rate with different PLL oscillation rate(For more details,

please refer to 5VT6126 DMPS *Application N*ote. HSS28G only integrates one PLL so that only 25G and 50G can co-existed in one HSS28G Macro.

The SmartPort™ group supported configuration modes are shown in the following table.

Table 4-1 : SmartPort™ Group Configuration in Octal SerDes Macro

Mode	SGMII	XFI	QSGMII	USXGMII	XLAUI
SerDes Lane 0	SGMII_0	XFI_0	QSGMII_0	USXGMII_0	XLAUI_0
SerDes Lane 1	SGMII_1	XFI_1	QSGMII_1	USXGMII_1	XLAUI_0
SerDes Lane 2	SGMII_2	XFI_2	QSGMII_2	USXGMII_2	XLAUI_0
SerDes Lane 3	SGMII_3	XFI_3	QSGMII_3	USXGMII_3	XLAUI_0
SerDes Lane 4	SGMII_4	XFI_4	QSGMII_4	USXGMII_4	XLAUI_1
SerDes Lane 5	SGMII_5	XFI 5	QSGMII_5	USXGMII_5	XLAUI_1
SerDes Lane 6	SGMII_6	XFI 6	QSGMII_6	USXGMII_6	XLAUI_1
SerDes Lane 7	SGMII_7	XFI 7	QSGMII_7	USXGMII_7	XLAUI_1

NOTE =

- 1. QSGMII/USXGMII can only be connected to the SerDes Lane0~11.
- 2. Typically, for dynamic switch application scenario, it is recommended to use 4 Lanes in HSS12G a total group, the speed of 4 lanes can be dynamic 5configured.

Table 4-2 : SmartPort™ Group Configuration in Quad SerDes Macro

Mode	SGMII	XFI	25G	XLAUI	50G	CAUI-4[1]
SerDes Lane 0	SGMII_0	XFI_0	25G_0	XLAUI_0	50G_0	CAUI_0
SerDes Lane 1	SGMII_1	XFI_1	25G_1			
SerDes Lane 2	SGMII_2	XFI_2	25G_2		50G_1	
SerDes Lane 3	SGMII_3	XFI_3	25G_3			

4.4 Typical Configuration

Table 4-3 : Typical Configuration

HSS Macro	16 x 10G + 2 x 40G	48x1G + 4x10G +2x40G	24 x 10G + 2 x 100G	24 x 10G + 8 x 25G
Octal SerDes Macro #0	XFI0 … XFI7	QSGMII0… QSGMII7	XFI0 … XFI7	XFI0 … XFI7
Octal SerDes Macro #1	XFI8 … XFI15	QSGMII8… QSGMII11 XFI0 … XFI3	XFI8 … XFI15	XFI8 … XFI15
Octal SerDes Macro #2			XFI16 … XF23	XFI16 … XF23
Quad SerDes Macro #0	XLAUI0	XLAUI0	CAUI0	25G0…25G3
Quad SerDes Macro #1	XLAUI1	XLAUI1	CAUI1	25G4…25G7

5 Memory Profile

5VT6126 incorporates eTCAM and eSRAM as table memory. FTM technology enables flexible table memory partition per customer requirement. Each table size combination is called as a “memory profile”.On chip memory resource ssuchas TCAM and embedded SRAM are considered as a sharing pool. With different memory profiles, the chip is able to support different cases such as more MAC address or more IP address. Table 5-1 shows example of memory profiles supported by 5VT6126.

Shared Buffer technology: to address the extra-large table size requirement in several special application scenarios, 5VT6126 integrates the shared buffer technology which allows the embedded packet buffer to be configured to work in packet store mode or Dynamic Tables mode. Shared buffer can be configured for the Dynamic Tables such as MacKey/MacAd/DsNexthop, etc. More details can be found in FTM related description of *5VT6126_Programmer’s_Guide_en.*

Table 5-1 : Typical 5VT6126 FTM™ Profiles

	MAX	Enterprise	IP RAN/ PTN
MAC	196K [Couple to 392K]	128K	16K
IP Host (v4/ v6)	112K	32K	8K/4K
IP LPM v4/v6	128K-192K [Worst-MAX.]	64K/16K	128K/ 32K
SCL (QinQ, VXLAN)	64K	32K	32K
MPLS	16K	8K	8K
Policer (IGS/EGS)	10K/2K	10K/2K	10K/ 2K
ACL	11.5K (8 Slices)	11.5K (8 Slices)	11.5K (8 Slices)
Buffer	9MB	4.5MB	9MB
Queue	4K	4K	4K
Counter	32K	32K	32K

6 System Interface

6.1 Overview

5VT6126 integrates the following major external interfaces:

- Multiple Speed SerDes links, Networkinterface
- I^2C interface to access the external OpticalModules
- PTP and Sync-E Interface for time synchronization and IEEE1588 protocol
- SMI, IEEE 802.3-compliant Serial Management Interface for communication with external PHYdevices
- LED interface: to control the operation of the LEDs on the frontpanel
- PCIE2.0
- CPU SubsystemInterface
  - DDR3/DDR4 SDRAM Interface, 16-bit + 8-bitECC
  - Quad Serial Peripheral Interface (QSPI) used by the CPU subsystem for boot and nonvolatilestorage
  - Serial Peripheral Interface (SPI) for CPU subsystem for low-speedaccess
  - USBInterface
  - SGMII Interface: two ports connected to external PHYs up to 1GE for management functionality.
  - GPIO 34 pins
  - SMI for external PHY management
  - EMMC interface for the communication with the external eMMC storage devices

NOTE

All interfaces need to be configured for normal operation.

6.2 Network Interface

5 HSS Macros are integrated in 5VT6126 to work as the network interfaces. Among these 5 HSS Macros, there are 3 Octal SerDes for 1.25G to 13G lane rate, and 2 Quad SerDes for 1.25G to 28.125G lane rate. These SerDes links support multiple speeds for multiple port standards, including the following industry standards interface (the baud rate also listed):

- 100BASE-FX, 1.25Gbps, only supported on HSS12.5G
- SGMII,1.25Gbps

- XAUI/10GBASE-KX4,3.125Gbps
- QSGMII,5Gbps*1
- USXGMII-Multiport, 5.15625Gbps*1
- XFI/SFI/10GBASE-KR/USXGMII-Multiport,10.3125Gbps*1
- DXAUI,6.25Gbps
- XLAUI/40GBASE-KR4/40GBASE-CR4,10.3125Gbps
- CAUI4/100GBASE-KR4/100GBASE-CR4,25.78125Gbps*2
- 25GAUI/25GBASE-KR/25GBASE-CR,25.78125Gbps*2
- 50GBASE-CR2/50GBASE-KR2,25.78125Gbps*2

*1: QSGMII and USXGMII are only supported by the 0~11 of 12.5G SerDes Lanes

*2: Only supported by 28G SerDes Macros

6.2.1 Interface Signals

Table 6-1 : Interface Signals

Pin Name	Type	Rate	Pin #	Description
HSS12G Group Interface				
HS_S[0:2]_REFCLK_P HS_S[0:2]_REFCLK_N	I LVDS	156.25MHz	6	HSS input differential clock, impedance 100±10% Ohm.
HS_S[0:2]_RX_N[0:7] HS_S[0:2]_RX_P[0:7]	I CML IN	1.25G~12.5Gbps	48	1.25G~12.5Gbps SerDes links input. Typical configurations are: • 100Base-FX • SGMII/1000BASE-X,1.25Gbps • XAUI/10GBASE-KX4, 3.125Gbps • QSGMII,5Gbps • Usxgmii-Multiport,5.15625Gbps • XFI/SFI/10GBASE-KR/USXGMII-Multiport, 10.3125Gbps • DXAUI,6.25Gbps • XLAUI/40GBASE-KR4/CR4, 10.3125Gbps
HS_S[0:2]_TX_N[0:7] HS_S[0:2]_TX_P[0:7]	O CML OUT	1.25G~12.5Gbps	48	1.25G~12.5Gbps SerDes links output.
HS_S[0:2]_REXT10K[1:2]	O LVCMOS	Static	6	Reserve Pins. Should be connected to via for factory debug.
HSS28G Group Interface				
CS_REFCLK_P CS_REFCLK_N	I LVDS	156.25MHz	2	Reference clock for 28G SerDes Macros

Pin Name	Type	Rate	Pin #	Description
CS_S[0:1]_RX[0:3]_P CS_S[0:1]_RX[0:3]_N	I CML IN	1.25G~28.125Gbps	16	1.25G~28Gbps SerDes links input • SGMII/1000BASE-X,1.25Gbps • XAUI/10GBASE-KX4, 3.125Gbps • QSGMII,5Gbps • Usxgmii-Multiport,5.15625Gbps • XFI/SFI/10GBASE-KR/USXGMII-Multiport, 10.3125Gbps • DXAUI,6.25Gbps • XLAUI/40GBASE-KR4/CR4, 10.3125Gbps • CAUI-4/100GBASE-KR4/CR4, 25.78125Gbps • 25GAUI/25GBASE-KR/CR, 25.78125Gbps • /50BASE-CR2/KR2, 25.78125Gbps
CS_S[0:1]_TX[0:3]_P CS_S[0:1]_TX[0:3]_N	O CML OUT	1.25G~28.125Gbps	16	1.25G~28Gbps SerDes links output
PCIe (HSS5G) Interface				
PCIE_REFCLK_P PCIE_REFCLK_N	I HCSL	100MHz	2	PCIE input deferential reference clock 100M.
PCIE_REXT	I LVCMOS	Static	1	External resistor for termination calibration: Connect 50 ohm external resistor (1% precision) between PCIE_REXT to AVDD18_PCIE (no need to be close to BGA BALL)
PCIE_RX_P PCIE_RX_N	I CML IN	2.5/5.0Gbps	2	PCIE lane input data.
PCIE_TX_P PCIE_TX_N	O CML OUT	2.5/5.0Gbps	2	PCIE lane output data.
PCIE_TPOUT	O LVCMOS	Static	1	Analog output test pin which is reserved for factory debug. It should be connected to a via.

6.2.2 USXGMII-M Interface

The Universal Serial Media Independent Interface for carrying multiple network ports over a single SerDes (USXGMII-M) is integrated in 5VT6126:

- Convey MULTIPLE network port soveran USXGMII MAC-PHY interface,e.g.:100M,1000M,1G, 2.5G,5G
- Utilize a 64/66 PCS to minimize power and serial bandwidth

- Use modified IEEE802.3 to add Alignment Markers to support multiple ports over single SerDes
- System Interface operates in full duplex modeonly

6.2.3 1GbE/2.5GbE Port

There are total 64 Multiple-Speed MACs integrated in 5VT6126 to provide up to 64x1GbE ports when the lane rate is working at 1.25G data rate. The embedded 1GE ports have the following features:

- IEEE 802.3zcompliance
- Support auto-negotiation withspeed
- Supports full duplex onlyoperations
- Supports full duplex flow control (IEEE802.3x)
- FCS generation for transmitting, checking for receivingpackets
- Includes PCS block (8b/10b @ QSGMII or SGMII) or (64b/66b @ USXGMII) for SerDes interface to external GigabitPHY

Basic Operation

5VT6126 implements a MAC unit with PCS layer integrated. It can be programmed to filter out frames that are longer or shorter than specific sizes.It also filters packets out with bad CRCs or receptionerror.

- Enable/DisablePort
- MAC Speed
- IEEE 802.3x FlowControl
- LinkState
- Enable/Disable CRCChecking
- Maximum Receive Unit(MRU)

The SerDes link runs at 3.125Gbps for 2500Mbps.

While SerDes link runs at 10.3125G for USXGMII-M interface，4 MACS will be connected to one SerDes link to receive and transmit data by the multiplexing function

While SerDes link runs at 5.0Gbps for QSGMII interface, 4 MACs will be connected to one SerDes link to receive and transmit data by the multiplexing function.

6.2.4 5GbE

5VT6126 also supports 5GbE port by USXGMII protocol. While data rate is 10.3125Gbps for USXGMII interface, 2 of 5G ports can receive and transmit data by the multiplexing function.

6.2.5 10GbEport

10 Gigabit MAC Standard Features

- Compliant to IEEE Std 802.3-2015 Clause46,47,48,49,72,73,74

10 Gigabit MAC Extended Features

- MAC/ RS/ PCS implementations compliant to IEEE 802.3specifications
- Comprehensive statistics gathering with statistic vector outputs
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IPG under all conditions and provides line rate performance
- XGMII link fault detection and generation
- Supports loopback for diagnose
- Supports backplane auto-negotiation and link training
- Supports Base-R FEC (FC (2112,2080))

Basic Operation

The SGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3-2015 including a MAC Control Sub-layer and PCS layer.

In transmitting direction,the SGMAC module receives data from internal databus and performs idle conversion,code group generation 64b/66b encoding for XFI/SFI/10G-KR.Next,the SGMAC prepares the data for transmission over one link for XFI/SFI/10G-KR/XAUI/DXAUI.

In receiving direction, the SGMAC module accepts 4-lane wide data for XAUI/DXAUI or 1-lane data for XFI/SFI/10G-KR from a SerDes lane.

6.2.6 40GbEPort

40 Gigabit MAC Standard Features

- Compliant to IEEE Std 802.3-2015 Clause 80~83

40 Gigabit MAC Extended Features

- MAC/RS/PCS implementations compliant to IEEE 802.3 specifications
- Supports flow-control in bothdirections
- Per frame and default programmable padding and FC Sinsertion
- XLGMII link fault detection andgeneration
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IPG under all conditions and provides line rate performance
- Supports backplane auto-negotiation and linktraining
- Supports Base-R FEC (FC (2112,2080))

Basic Operation

The XLGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3ba.

In transmitting direction, the XLGMAC module receives data from internal data bus and performs idle conversion, code group generation, and 64b/66b encoding for XLAUI. After that, the XLGMAC prepares the data for transmission over 4 links for XLAUI.

In receiving direction, the XLGMAC module accepts 4-lane wide data for XLAUI from four lines of SerDes. XLGMAC pass data to 64b/66b decoding, then go to the XLGMII data bus

During operation, the XLGMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.7 25GbE Port

25 Gigabit MAC Standard Features

- Compliant to IEEEStd802.3by
- Compliant to 25G&50G Ethernet Consortium Specification Rev1.6

25 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to IEEE 802.3 by and 25G&50G Consortium specifications
- Supports both RS-FEC (RS (528,514)) and Base-R FEC (FC(2112,2080))
- Supports flow-control in both directions
- Per frame and default programmable padding and FC Sinsertion
- 25GMII link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IPG under all conditions and provides line rate performance
- Supports IEEE Clause 73 backplane auto-negotiation and link training

Basic Operation

The 25GMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3by or 25G&50G Consortium.

In transmitting direction, the 25GMAC module receives data from internal data bus and performs idle conversion,code group generation,and64b/66 bencoding for 25GAUI.Afterthat, the 25GMAC prepares the data for transmission over one link for25GAUI.

In receiving direction, the 25GMAC module accepts one lane data for 25GXAUI from one line of SerDes. 25GMAC pass data to 64b/66b decoding, then go to the 25GMII data bus.

During operation, the 25GMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.8 50Gb EPort

50 Gigabit MAC Standard Features

- Compliant to 25G&50G Ethernet Consortium SpecificationRev1.6

50 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to 25G&50G Consortium specifications
- Supports both RS-FEC (RS (528,514)) and Base-R FEC (FC(2112,2080))
- Supports flow-control in bothdirections
- Per frame and default programmable padding and FCSinsertion
- 50GMII link fault detection andgeneration
- Supports Deficit Idle Count for maximum data throughput
- Maintains minimum IPG under all conditions and provides line rate performance
- Support 25G&50G Consortium backplane auto-negotiation and link training

Basic Operation

The 50GMAC module performs the packet transmission and reception protocol as described in 25G&50G Consortium.

In transmitting direction, the 50GMAC module receives data from internal data bus and perform sidle conversion,code group generation,and 64b/66 bencoding for 50GAUI.After that, the 50GMAC prepares the data for transmission over two links for 50GAUI.

In receiving direction,the 50GMAC module accept s2-lanewide data for 50GXAUI from two lines of SerDes. 50GMAC pass data to 64b/66b decoding, then go to the 50GMII databus.

During operation, the 50GMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.2.9 100Gb EPort

100 Gigabit MAC Standard Features

- Compliant to IEEE Std802.3-2015 Clause80,81,82,83,91,92,93

100 Gigabit MAC Extended Features

- MAC/RS/PCS/FEC implementations compliant to IEEE 802.3specifications
- Supports 100G RS-FEC (RS(528,514))
- Supports flow-control in both directions
- Per frame and default programmable padding and FCS insertion
- CGMII link fault detection and generation
- Supports Deficit Idle Count for maximum data throughput

- Maintains minimum IPG under all conditions and provides line rate performance
- Supports backplane auto-negotiation and link training

Basic Operation

The CGMAC module performs the packet transmission and reception protocol as described in IEEE standard 802.3ba.

In transmitting direction,the CGMAC module receives data from internal databus and performs idle conversion,code group generation,and 64b/66b encoding for CAUI.After that,the CGMAC prepares the data for transmission over 4 links forCAUI.

In receiving direction, the CGMAC module accepts 4-lane wide data for CAUI from four lines of SerDes. CGMAC pass data to 64b/66b decoding, then go to the CGMII data bus.

During operation, the CGMAC collects statistics about the success and failure of various operations. The statistic information is processed by network management entities in the system.

6.3 CPU Interface

The feature sets of 5VT6126 CPU Subsystem within the switch device are listed as below.

- Onedual-core ARM A53CPU runningat1.2GHz or 800MHz,which can be configured by the chip pin, with the following caches:
  - 32KB L1 Instruction cache and 32KB L1 datacache
  - Internal 256 KB L2Cache
- Neon + FPU for float point computing
- 96KB RAM on system AXIbus
- 64KB Boot ROM on system AXIbus
- 16-bit + 8bit (ECC) wide configuration DDR3/DDR4 interface
- USB2.0 Interface
- 34GPIOs
- 2 SGMII Interfaces for out-of-band management
- SMI Interface
- EMMC interface support4.51
- QSPI with two CS signals, support 1-bit, 2-bit, and 4-bit workmode
- SPI interface with four CSsignals
- Security boot uptechnology
- 2 I^2C SoC Interface to connect the I^2C device between internal CPU and external I^2Cdevices

6.4 PCIe Interface

The single SerDes lane is dedicated for CPU interface connection. The PCIE could be used for register configuration, DMA for internal table access, and packet I/O.

Also, if internal CPU is enabled, PCIe interface can be configured to work at Endpoint mode or Rootport mode.

- **Rootport mode**: PCIe interface can be controlled by the internal CPU for the connection with the external PCIedevices;
- **Endpoint mode:** Another external CPU can be connected to the PCIe interface for switch control.When 5VT6126 work sin Endpoint mode, 5VT6126 need store lease reset(RST_SUP_B) 5ms earlier than externalCPU.

5VT6126 PCIE supports Gen1 and Gen2 protocol, it provides maximum data rate of 5Gbps. The datarate is auto-negotiated during PCIE training.It is recommended that 5VT6126 and external CPU use the same originclock.

6.5 I²C Master Interface

5VT6126 I²C Master Interface supports serial bus interface which is compatible with Philips I²C standards. But it can only run at master mode and no more than 400Kbps.

The switch core I²C master interfaces do not support clock synchronizing function and can only be used to access the external optical modules such as SFP, XFP, SFP +. The state of external optical modules could be collected by I²C master interface periodically and save to internal 384 Bytes memory.

6.6 I²C Slave Interface

5VT6126 I²C slave interface supports serial bus interface which is compatible with Philips I²C standards. But it can only run at slave mode and no more than 400Kbps.

The I²C slave interface is used for slow speed configuration for internal register or table. In most cases, the I²C slave interface is used to configure and debug the PCIE interface.

The address LSB 2 bits of 5VT6126 I²C slave interface is configurable by tie 2 external pins to VDD or GND. So the I²C slave address is 7'b011_11??. For 7bits address mode and for 10 bits address mode, the address is 10'b00_0011_11??.

6.7 PTP and Sync Ethernet Interface

5VT6126 supports packet-based Time Synchronization (IEEE1588 and IEEE802.1AS) and Synchronous Ethernet Layer-one Clock Recovery (ITU G.8261). The synchronous communication over Ethernet is a control protocol that negotiates resource and timing on the network. The protocol synchronizes the real-time clocks in a system and enables network measurement and control based on real time.

6.7.1 Sync Ethernet Interface

The sync Ethernet interface provides the scheme to recover the clock from upstream devices and pass the clock to downstream devices through physical layer. 5VT6126 generates three output clocks to feed in an external DPLL to produce transmitting reference clock.

Figure 6-1 shows the detail of one instance of recovery clock and how the recovery clock transfer to transmitting reference clock.

In typical application cases, the output selected recovery clock should be guarded by the corresponding link state of MAC and SerDes. 5VT6126 also has the valid output to provide the capability for customer to shut off the selected recovery clock off chip while the corresponding link state of MAC or SerDes is failure.

Figure 6-1 : Sync Ethernet Clock Scheme

Table 6-2 : Sync Ethernet Signals

Name	IO	Description
RECV_CLK[0:2]	O, CMOS	SyncE recovery Clock

5VT6126 supports clock recovering via SerDes. The recovered clock can be divided by divider, which has a range of 1 to 1024. Each output can be controlled by link status of the recovery path. The detailed recovery clock frequency of different port speed is as bellow table.

Table 6-3 : Recovery Clock Frequency of Different port speed

SerDes Type	Mode	Data Rate (Gbps)	Recovery clock Frequency (MHz)	Divider	Output Clock Frequency (MHz)
HSS12.5G	SGMII	1	125	64	1.953125
HSS12.5G	SGMII	2.5	312.5	160	1.953125
HSS12.5G	XFI/XLG	10	322.265625	165	1.953125
HSS28G	SGMII	1	39.0625	20	1.953125
HSS28G	SGMII	2.5	97.65625	50	1.953125
HSS28G	XFI/XLG	10	322.265625	165	1.953125
HSS28G	25G/50G/100G	25	805.6640625	825	0.9765625

6.7.2 PTP Interface Signals

The PTP signals provide three types of signals. The first one is the differential reference clock fed into the internal TsEngine. The second one is the sync interface which is used for receiving time code (Slave Mode) or transmitting time code and synthesized output low speed TDM clock (Master Mode). The last one is the ToD signal to receive or transmit time code which obeys the China Mobile's standards.

Table 6-4 : PTP signals

Pin Name	Type	Description
PTP_REFCLK_P PTP_REFCLK_N	I LVDS	TsEngine Differential clock input, typical frequency is 125MHz
SYNC_CLK	I/O LVCMOS	TsEngine sync clock, up to 25MHz.
SYNC_PULSE	I/O LVCMOS	TsEngine sync pulse.
SYNC_CODE	I/O LVCMOS	TsEngine sync code.
TOD_CODE	I/O LVCMOS	ToD (Time of Date) output code, typical rate is 9600 baud rate.
TOD_PULSE	I/O LVCMOS	ToD output pulse, typical 1pps pulse
TOD_REFCLK	I LVCMOS1.8V	ToD Reference Clock, typical 96MHz

6.8 SMI Interface

6.8.1 SMI Interface Signals

5VT6126 supports the IEEE 802.3 MII Management Interface via the MDIO and MDC pins. MDIO is a serial input and output data signal which is clocked by the periodic clock MDC. This interface allows 5VT6126 accesses to the PHY internal registers, by which 5VT6126 can monitor and control the real-time status of the external PHY devices connected to 5VT6126.

Besides,SMI interface could scan the state of PHY devices continuous ly without CPU involved to collect the link status. It will trigger the APS operation while there are failures oflinks.

Table 6-5 : SMI Interface Signals

Name	IO	Description
MDC_A[1:0] MDC_B[1:0]	O LVCMOS	External PHI MDIO clock, compatible with 1GE PHY and 10GE PHY.
MDIO_A[1:0] MDIO_B[1:0]	I/O LVCMOS	External PHY MDIO data, compatible with 1GE PHY and 10GE PHY.

6.8.2 Operation

Though each SMI interface can support up to 32 PHY devices, 5VT6126 provides 2 groups (SMI A/B) to mitigate the load to reduce the system design difficulty. Each group, includes 2 interfaces, can be configured as either 10G or 1G MDIO mode. For example, the MDIO_A_0 and MDIO_A_1 need to be configured to 10G or to 1G at the same time.

There are two operation types for SMI interface operation,the one is read/write operation,the other is auto-scan. The read/write operation can only access one register one time, but the auto-scan can access multiple status registers of many PHY.

6.9 MAC LED Interface

The serial LED interface consists of encoded bit stream. The timing and encoding diagram are shown in the following figure.An EPL Dorsimple shift register logic is needed to convert this bit stream to drive individual lLED.

The port sequence is programmable through internal register. Every port supports 2 modes: On/Off mode and Blink mode.Everyport can be configured to support 1 mode(onlyoneLEDfor one MAC) or 2 modes (there are 2 LEDs for one MAC) independently. If mode 1 is configured, then this portonly output 1bit on LED interface;If mode2 is configured,then this port output 2 continual bits on LED interface.

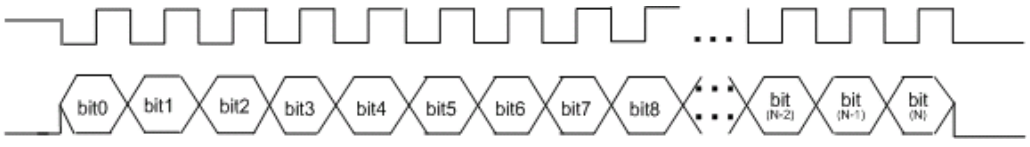

Figure 6-2 : LED Interface Timing and Encoding Explanation

6.9.2 LED Interface Signals

5VT6126 provides a pair of LED interfaces according to SmartPort™ Group. The LED interface signals are given as bellow:

Table 6-6 : LED Interface Signals

Name	IO	Description
LED_CLK	O, LVCMOS	LED Clock
LED_DATA	O, LVCMOS	Encoded bit stream to drive LED

6.9.3 LED Bit Stream EncodeModes

In order to maximize the facility of driving LED under different application scenario, total ten LED bit stream encode modes are supported in 5VT6126 this could save the external glue logic and only the shift logic is needed.

Table 6-7 : LED Bit Stream Encode Modes

Mode #	Mode Description	On/Off	Blink
0	RX Link	RX Link = 1/0	0
1	TX Link (10GE only)	TX Link = 1/0	0
2	RX Link and activity	RX Link = 1/0	RX activity
3	TX Link and Activity (10GE only)	TX Link = 1/0	TX activity
4	RX Link and RX/TX activity	RX Link = 1/0	RX or TX activity
5	TX activity	0	TX activity
6	RX activity	0	RX activity
7	RX/TX activity	0	RX or TX activity
8	LED Force On	1	0
9	LED Force Off	0	0

So, there are one pair of 2bits (total 4 bits) stand for the LED mode. For example, if user wants LED to be configured to work at mode #2 (Rx Link and activity), LED On/Off mode encode should be 2'b01, LED blink mode encode should be 2'b01.

The LED control are 2 bits, which are deduced from the LED On/Off mode and LED blink mode encoding, LED_PortStatus[1:0] MSB bit is blink bit, 1'b1 is blinking, 1'b0 is Non-blinking; on the other hand, LED_PortStatus[1:0] LSB bit is On/Off bit, 1'b1 is On, 1'b0 is Off. Besides, the MSB bit (i.e. the LED blinking bit) has the higher priority than LSB bit.

Take LED mode #2 as an example:

(1) Cfg LED On/Off mode encode = 2'b01, LED blink mode encode=2'b01;

(2) IfsampletheRxLinkstatus=1,thensetLED_PortStatus[0]=1'b1;IfsampletheRxactivity status = 1, then set LED_PortStatus[1]=1'b1.

(3) Since LED_PortStatus[1:0]= 2'b11, and blink status has the higher priority, the LED refresh bit stream will be 0 => 1 => 0 => 1 toggling according to the interval of LEDrefresh.

The LED blink behavior is implemented through the "and" operation of BLINK square-wave and the BLINK bit of LED_PortStatus.

If need secondary LED for one port, such as 10GE port, the primary LED displays "Rx Link and activity" (LED mode #2), and the secondary LED displays "TX Link and activity" (LED mode #3), then an extra LED port status bits are required.

Note that if the customer needs all of the MACs' raw link and activity status to be output for further processing (LedRawStatusCfg.rawStatusEn), all of the MACs' mode configuration are not effective.

7 Pin-Map and Pin-Outtable

This section provides the pin map and pin-out table with pin assignment for 5VT6126.

7.1 5VT6126 PinMap

Table 7-1 : 5VT6126 Pin Map Top View Column 1-6

	1	2	3	4	5	6
A	VSS	VSS	DDR_DQ4	DDR_DM0	VSS	HS_RX_P0
B	VSS	VDDIO_DDR	DDR_DQ3	DDR_DQ6	VSS	HS_RX_N0
C	DDR_DQS_N0	DDR_DQS_P0	DDR_DQ2	DDR_DQ5	VSS	VSS
D	DDR_DQ7	DDR_DQ1	DDR_DQ0	VDDIO_DDR	VSS	VSS
E	DDR_DM1	DDR_DQ12	DDR_DQ13	DDR_DQ11	VDDIO_DDR	VSS
F	VSS	VDDIO_DDR	DDR_DQ14	DDR_DQ10	VSS	VSS
G	DDR_DQS_P1	DDR_DQS_N1	DDR_DQ9	DDR_DQ15	VSS	VDDIO_DDR
H	DDR_DQ18	DDR_DM2	DDR_DQ8	VDDIO_DDR	VSS	VDDIO_DDR
J	DDR_DQ16	DDR_DQ20	DDR_DQ23	DDR_DQ22	VSS	VDDIO_DDR
K	DDR_DQS_P2	DDR_DQS_N2	DDR_DQ19	DDR_DQ21	VSS	VDDIO_DDR
L	VSS	VDDIO_DDR	DDR_DQ17	VDDIO_DDR	VSS	VDDIO_DDR
M	DDR_CLK_N0	DDR_CLK_P0	DDR_ODT2	DDR_CKE2	DDR_CS_B3	VDDIO_DDR
N	VSS	VDDIO_DDR	DDR_CS_B1	DDR_ODT0	VSS	VDDIO_DDR
P	DDR_CLK_N1	DDR_CLK_P1	DDR_CKE0	DDR_ODT1	VSS	VDDIO_DDR
R	DDR_CAS_B	DDR_ADDR14	DDR_CS_B0	DDR_CKE1	VSS	VDDIO_DDR
T	DDR_RAS_B	DDR_WE_B	DDR_CKE3	DDR_CS_B2	VSS	VDDIO_DDR
U	DDR_ADDR10	DDR_ADDR12	VSS	VDDIO_DDR	DDR_ODT3	VDDIO_DDR
V	DDR_BA2	DDR_ADDR15	DDR_BA1	DDR_ADDR2	VSS	VDDIO_DDR
W	DDR_ADDR4	DDR_ADDR3	DDR_ADDR6	DDR_ADDR9	VSS	VDDIO_DDR
Y	DDR_TEN	DDR_BA0	VSS	VDDIO_DDR	DDR_PAR	VDDIO_DDR
AA	DDR_ADDR1	DDR_ADDR0	DDR_ADDR5	DDR_ADDR8	DDR_RST_B	VDDIO_DDR
AB	DDR_ADDR7	DDR_ADDR13	DDR_ADDR11	DDR_ALERT_B	DDR_ZQ	VDDIO_DDR
AC	VSS	VSS	VSS	VSS	USB_D_P	USB_D_N
AD	USB_TXR_TUNE	USB_ID0	USB_VBUS0	VSS	VSS	VSS
AE	VSS	VSS	VSS	VSS	HS_S0_TX_P1	HS_S0_TX_N1

	1	2	3	4	5	6
AF	HS_S0_TX_N0	HS_S0_TX_P0	VSS	HS_S0_TX_N2	HS_S0_TX_P2	VSS
AG	VSS	VSS	VSS	VSS	VSS	VSS
AH	HS_S0_RX_N0	HS_S0_RX_P0	VSS	VSS	HS_S0_TX_P3	HS_S0_TX_N3
AJ		HS_S0_RX_N1	HS_S0_RX_P1	VSS	VSS	HS_S0_TX_P4
AK	VSS	VSS	VSS	VSS	VSS	VSS
AL	HS_S0_RX_P2	HS_S0_RX_N2	VSS	HS_S0_TX_N5	VSS	HS_S0_TX_P6
AM	VSS	VSS	VSS	HS_S0_TX_P5	VSS	HS_S0_TX_N6
AN	HS_S0_RX_P3	HS_S0_RX_N3	VSS	VSS	VSS	VSS
AP	VSS	VSS	VSS	VSS	VSS	VSS
AR	HS_S0_RX_N4	VSS	VSS	VSS	HS_S0_RX_P6	VSS
AT	HS_S0_RX_P4	VSS	HS_S0_RX_N5	VSS	HS_S0_RX_N6	HS_S0_RX_P7
AU	VSS	VSS	HS_S0_RX_P5	VSS		HS_S0_RX_N7

Table 7-2 : 5VT6126 Pin Map Top View Column 7-12

	7	8	9	10	11	12
A	VSS	HS_RX_P1	VSS	VSS	AVSS_PCIE	PCIE_TX_P
B	VSS	HS_RX_N1	VSS	VSS	AVSS_PCIE	PCIE_TX_N
C	HS_TX_P0	VSS	HS_TX_P1	VSS	AVSS_PCIE	AVSS_PCIE
D	HS_TX_N0	VSS	HS_TX_N1	VSS	AVSS_PCIE	AVSS_PCIE
E	VSS	VSS	VSS	VSS	AVSS_PCIE	AVSS_PCIE
F	VSS	HS_CMU_REFCLK_P	VSS	VSS	PCIE_REFCLK_P	AVSS_PCIE
G	VSS	HS_CMU_REFCLK_N	VSS	VSS	PCIE_REFCLK_N	AVSS_PCIE
H	VSS					
J	VSS					
K	VSS				HS_CMU_REXT 10K	AVDD09_VCO_HS3
L	VSS				VSS	VSS
M	VSS				AVDD18_HS3	AVDD18_HS3
N	VSS				VSS	AVDD09_HS3
P	VSS				AVDD18_DATA_L16_DDR	AVSS18_DATA_L16_DDR
R	VSS				DDR_VREF1	DDR_VREF0
T	VSS				AVDD18_DATA_H8_DDR	AVSS18_DATA_H8_DDR
U	VSS				VSS	VSS
V	VSS				AVSS18_ADD_	AVDD18_ADD_

	7	8	9	10	11	12
					DDR	DDR
W	VSS				VSS	VSS
Y	VSS				AVDD33_USB	VDD
AA	VSS				VDD_USB	VSS
AB	VSS				AVDD33_USB	VDD
AC	VSS				VSS	VSS
AD	VSS				VDD	VDD
AE	VSS				VSS	VSS
AF	VSS				AVDD09_HS0	AVDD09_HS0
AG	VSS				HS_S0_CMU1_REXT10K	VSS
AH	VSS				HS_S0_CMU2_REXT10K	AVDD18_HS0
AJ	HS_S0_TX_N4					
AK	VSS					
AL	VSS	VSS	HS_S1_TX_N8	VSS	VSS	HS_S1_TX_P10
AM	HS_S0_TX_P7	VSS	HS_S1_TX_P8	HS_S1_TX_N9	VSS	HS_S1_TX_N10
AN	HS_S0_TX_N7	VSS	VSS	HS_S1_TX_P9	VSS	VSS
AP	VSS	VSS	VSS	VSS	VSS	VSS
AR	VSS	HS_S1_RX_N8	VSS	VSS	HS_S1_RX_P10	VSS
AT	VSS	HS_S1_RX_P8	HS_S1_RX_N9	VSS	HS_S1_RX_N10	HS_S1_RX_P11
AU	VSS		HS_S1_RX_P9	VSS		HS_S1_RX_N11

Table 7-3 : 5VT6126 Pin Map Top View Column 13-18

	13	14	15	16	17	18
A	AVSS_PCIE	PCIE_RX_P	AVSS_PCIE	VDD	VDD	
B	AVSS_PCIE	PCIE_RX_N	AVSS_PCIE	VDD	VDD	THM_VINS0
C	AVSS_PCIE	AVSS_PCIE	VSS	VDD	VDD	THM_VREFP
D	PCIE_TPOUT	PCIE_REXT	VSS	VDD	VDD	VSS
E	AVSS_PCIE	VSS	VSS	VDD	VDD	VDD
F	CORE_REFCLK_P	VSS	PTP_REFCLK_P	VDD	VDD	VDD
G	CORE_REFCLK_N	VSS	PTP_REFCLK_N	VSS	VDD	VDD
H						
J						

	13	14	15	16	17	18
K	AVSS_PCIE	AVSS_PCIE	AVSS_PCIE	AVDD18_THM	VDD	VDD
L	AVSS_PCIE	AVDD09_VCO_PCIE	AVDD18_PCIE	VSS	VDD	VDD
M	AVDD18_HS3	AVDD09_HS3	AVSS_PCIE	VDD	VDD	VDD
N	AVDD09_HS3	VSS	AVDD09_PCIE	VSS	VDD	VSS
P	VDDIO_DDR	VDD	VSS	VDD	VSS	VDD
R	VDDIO_DDR	VSS	VDD	VSS	VDD	VSS
T	VDDIO_DDR	VDD	VSS	VDD	VSS	VDD
U	VDDIO_DDR_CK	VSS	VDD	VSS	VDD	VSS
V	VDDIO_DDR	VDD	VSS	VDD	VSS	VDD
W	VDD	VSS	VDD	VSS	VDD	VSS
Y	VSS	VDD	VSS	VDD	VSS	VDD
AA	VDD	VSS	VDD	VSS	VDD	VSS
AB	VSS	VDD	VSS	VDD	VSS	VDD
AC	VDD	VSS	VDD	VSS	VDD	VSS
AD	VSS	VDD	VSS	VDD	VSS	VDD
AE	VDD	VSS	AVDD09_VCO_HS0	VSS	VDD	VSS
AF	AVDD09_HS0	AVDD09_HS0	VSS	VSS	AVDD09_HS1	AVDD09_HS1
AG	VSS	VSS	VSS	VSS	VSS	VSS
AH	AVDD18_HS0	AVDD18_HS0	AVDD18_HS0	HS_S1_CMU1_REXT10K	VSS	AVDD18_HS1
AJ						
AK						
AL	VSS	VSS	VSS	VSS	VSS	VSS
AM	HS_S1_TX_P11	VSS	HS_S1_TX_N12	VSS	VSS	HS_S1_TX_N14
AN	HS_S1_TX_N11	VSS	HS_S1_TX_P12	HS_S1_TX_N13	VSS	HS_S1_TX_P14
AP	VSS	VSS	VSS	HS_S1_TX_P13	VSS	VSS
AR	VSS	VSS	VSS	VSS	VSS	VSS
AT	VSS	HS_S1_RX_N12	VSS	HS_S1_RX_N13	VSS	HS_S1_RX_N14
AU	VSS	HS_S1_RX_P12	VSS	HS_S1_RX_P13	VSS	HS_S1_RX_P14

Table 7-4 : 5VT6126 Pin Map Top View Column 19-24

	19	20	21	22	23	24
A	MSH_DATA2	MSH_DATA7		QSPI_DATA2	TDI	
B	MSH_DATA1	MSH_DATA6	QSPI_DATA0	QSPI_DATA3	TMS	TDO
C	MSH_DATA0	MSH_DATA5	VSS	QSPI_CLK	TCK	VSS
D	MSH_CMD	MSH_DATA4	QSPI_DATA1	QSPI_CS0	SD_SW_VOLT_EN	MSCL0
E	MSH_CLK	MSH_DATA3	MSH_RST_B	QSPI_CS1	SD_DET_B	MSDA0
F	VSS	VSS	VSS	SD_WP	VSS	VSS
G	VDD	VSS	VDDIO18_EFUSE_MEM	VDDIO18_EFUSE_INFO	VSS	VSS
H						
J						
K	AVDD18_DDRPLL	VDD09_DDRPLL	AVDD18_PLL	AVDD18_LVDS	VSS	VSS
L	AVSS_DDRPLL	VSS_DDRPLL	AVSS_PLL	VSS	VDDOUT_MSH	VDDOUT_G5
M	VSS	VDD	VSS	VDD	VSS	VDD
N	VDD	VSS	VDD	VSS	VDD	VSS
P	VSS	VDD	VSS	VDD	VSS	VDD
R	VDD	VSS	VDD	VSS	VDD	VSS
T	VSS	VDD	VSS	VDD	VSS	VDD
U	VDD	VSS	VDD	VSS	VDD	VSS
V	VSS	VDD	VSS	VDD	VSS	VDD
W	VDD	VSS	VDD	VSS	VDD	VSS
Y	VSS	VDD	VSS	VDD	VSS	VDD
AA	VDD	VSS	VDD	VSS	VDD	VSS
AB	VSS	VDD	VSS	AVDD18_CS	AVDD18_CS	AVDD18_CS
AC	VDD	VSS	VDD	VSS	VSS	VSS
AD	VSS	VDD	VSS	VDD	VDD	VDD
AE	AVDD09_VCO_HS1	VSS	VDD	VSS	AVDD09_VCO_HS2	VSS
AF	VSS	AVDD09_HS1	AVDD09_HS1	VSS	VSS	AVDD09_HS2
AG	AVDD18_HS1	VSS	VSS	VSS	VSS	VSS
AH	AVDD18_HS1	AVDD18_HS1	VSS	HS_S1_CMU2_REXT10K	AVDD18_HS2	AVDD18_HS2
AJ						
AK						
AL	HS_S1_TX_P15	VSS	VSS	HS_S2_TX_P17	VSS	VSS
AM	HS_S1_TX_N15	VSS	HS_S2_TX_P16	HS_S2_TX_N17	VSS	HS_S2_TX_N

	19	20	21	22	23	24
						18
AN	VSS	VSS	HS_S2_TX_N16	VSS	VSS	HS_S2_TX_P18
AP	VSS	VSS	VSS	VSS	VSS	VSS
AR	HS_S1_RX_P15	VSS	VSS	HS_S2_RX_N17	VSS	VSS
AT	HS_S1_RX_N15	VSS	HS_S2_RX_P16	HS_S2_RX_P17	VSS	HS_S2_RX_N18
AU		VSS	HS_S2_RX_N16		VSS	HS_S2_RX_P18

Table 7-5 : 5VT6126 Pin Map Top View Column 25-30

	25	26	27	28	29	30
A	SCL_SOC0	SDA_SOC1		MDIO_B0	MDC_SOC	
B	SDA_SOC0	SCL_SOC1	MDIO_A0	MDC_B0	MDIO_SOC	GPIOHS1
C	TRST_B	MDC_A0	VSS	GPIO5	GPIO4	VSS
D	MSDA1	MDIO_B1	GPIO2	GPIO3	GPIO7	GPIOHS0
E	MSCL1	MDIO_A1	MDC_B1	GPIO0	GPIO6	GPIOHS11
F	VSS	MDC_A1	VSS	GPIO1	VSS	GPIOHS10
G	VSS	VSS	VSS	VSS	VSS	VSS
H						
J						
K	VDDIO3318_MSH	VDDIO3318_MSH	VDDIO33			
L	VDDIO18	VDDIO18	VDDIO33			
M	VSS	VDDOUT_MDIO_A	VDDIO3312_MDIO_A			
N	VDD	VDDOUT_MDIO_B	VDDIO3312_MDIO_B			
P	VSS	VDDIO18	VDDIO3318_GPIO_7_0			
R	VDD	VDDIO18	VDDOUT_GPIO_7_0			
T	VSS	VDDIO18	VDDIO33			
U	VDD	VDDOUT_G1	VDDIO33			
V	VSS	VDDOUT_G2	VDDIO33			
W	VDD	VDDOUT_G3	VDDIO33			
Y	VSS	VDDOUT_G4	VDDIO33			
AA	VDD	VDDOUT_RECV	VDDIO3318_RECV			

	25	26	27	28	29	30
AB	AVDD18_CS	AVDD18_CS	AVDD18_CS			
AC	VSS	VSS	VSS			
AD	VDD	VDD	VDD			
AE	VDD	VSS	VSS			
AF	AVDD09_HS2	AVDD09_HS2	AVDD09_HS2			
AG	VSS	VSS	HS_S2_CMU2_REXT10K			
AH	AVDD18_HS2	AVDD18_HS2	HS_S2_CMU1_REXT10K			
AJ						
AK						
AL	HS_S2_TX_N19	VSS	VSS	HS_S2_TX_P21	VSS	VSS
AM	HS_S2_TX_P19	VSS	HS_S2_TX_P20	HS_S2_TX_N21	VSS	HS_S2_TX_N22
AN	VSS	VSS	HS_S2_TX_N20	VSS	VSS	HS_S2_TX_P22
AP	VSS	VSS	VSS	VSS	VSS	VSS
AR	HS_S2_RX_N19	VSS	VSS	HS_S2_RX_P21	VSS	VSS
AT	HS_S2_RX_P19	VSS	HS_S2_RX_P20	HS_S2_RX_N21	VSS	HS_S2_RX_N22
AU		VSS	HS_S2_RX_N20		VSS	HS_S2_RX_P22

Table 7-6 : 5VT6126 Pin Map Top View Column 31-37

	32	33	34	35	36	37
A	GPIOHS5		GPIOHS8	DEBUG_MODE0	VSS	VSS
B	GPIOHS4	GPIOHS6	GPIOHS7	DEBUG6	DEBUG_MODE1	VSS
C	GPIOHS3	VSS	GPIOHS9	DEBUG5	WDT1_RST_B	WDT0_RST_B
D	GPIOHS13	GPIOHS2	DEBUG3	DEBUG7	USB_OVC_B	CFG_GPIO_SEL
E	VSS	DEBUG0	DEBUG1	VSS	RST_SUP_B	
F	DEBUG2	DEBUG_MODE2	DEBUG4	CFG_PLL_SUP_BYP	UART_TXD0	UART_RXD0
G	VSS	TOD_REFCLK	CFG_PLL_CORE_BYP	UART_RXD2	UART_TXD1	UART_RXD1
H	BOOT_LPBK_TEST_MODE	BOOT_USB_VREG_BYP	BOOT_I2C_SA1	VSS	UART_TXD2	
J	VSS	BOOT_CPU_DIS	BOOT_I2C_SA0	BOOT_PCIE_RP_MODE	BOOT_PCIE_FORCE_MODE	BOOT_PCIE_AUTO_MODE
K	BOOT_CPU_SPEED	BOOT_STRAP0	BOOT_RESV3	BOOT_RESV1	BOOT_RESV2	BOOT_RESV0
L	VSS	BOOT_STRAP1	BOOT_STRAP2	VSS	BOOT_TEST_M	

	32	33	34	35	36	37
					ODE	
M	VSS	GPIO9	GPIO12	GPIO11	GPIO10	GPIO13
N	GPIO8	LED_CLK	LED_DATA	FUSE_DONE	GPIO14	GPIO15
P	VSS	INTR_B1	INTR_B0	VSS	FUSE_FAIL	
R	VSS	INTR_B2	INTR_B3	SYNC_CLK	SYNC_PULSE	SYNC_CODE
T	TOD_PULSE	TOD_CODE	RECV_CLK0	VSS	RECV_CLK1	RECV_CLK2
U	VSS	VSS	VSS	VSS	VSS	VSS
V	HS_S2_REFCLK_P	VSS	VSS	HS_S1_REFCLK_N	HS_S1_REFCLK_P	
W	HSS_REFCLK_P	HSS_REFCLK_N	VSS	VSS	HS_S0_REFCLK_N	HS_S0_REFCLK_P
Y	VSS	VSS	VSS	VSS	VSS	VSS
AA	VSS	CS_REFCLK_N	CS_REFCLK_P	VSS	CS_S1_RX_N7	CS_S1_RX_P7
AB	VSS	VSS	VSS	VSS	VSS	VSS
AC	VSS	CS_S1_TX_P7	CS_S1_TX_N7	VSS	CS_S1_RX_N5	CS_S1_RX_P5
AD	VSS	VSS	VSS	VSS	VSS	VSS
AE	VSS	CS_S1_TX_N5	CS_S1_TX_P5	VSS	CS_S1_RX_N6	CS_S1_RX_P6
AF	VSS	VSS	VSS	VSS	VSS	VSS
AG	VSS	CS_S1_TX_P6	CS_S1_TX_N6	VSS	CS_S1_RX_P4	CS_S1_RX_N4
AH	VSS	VSS	VSS	VSS	VSS	VSS
AJ	VSS	CS_S1_TX_P4	CS_S1_TX_N4	VSS	CS_S0_RX_P3	CS_S0_RX_N3
AK	VSS	VSS	VSS	VSS	VSS	VSS
AL	VSS	CS_S0_TX_P3	CS_S0_TX_N3	VSS	CS_S0_RX_P0	CS_S0_RX_N0
AM	VSS	VSS	VSS	VSS	VSS	VSS
AN	VSS	CS_S0_TX_P0	CS_S0_TX_N0	VSS	CS_S0_RX_P2	CS_S0_RX_N2
AP	VSS	VSS	VSS	VSS	VSS	VSS
AR	VSS	CS_S0_TX_N2	CS_S0_TX_P2	VSS	CS_S0_RX_P1	CS_S0_RX_N1
AT	VSS	VSS	VSS	VSS	VSS	VSS
AU	VSS	CS_S0_TX_P1	CS_S0_TX_N1	VSS	VSS	VSS

7.2 5VT6126 Pin-OutTable

Table 7-7 : 5VT6126 Pin-Out Table (by Ball)

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A1	VSS	E31	GPIOHS16	V33	VSS
A10	VSS	E32	VSS	V34	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A11	AVSS_PCIE	E33	DEBUG0	V35	HS_S1_REFCLK_N
A12	PCIE_TX_P	E34	DEBUG1	V36	HS_S1_REFCLK_P
A13	AVSS_PCIE	E35	VSS	V4	DDR_ADDR2
A14	PCIE_RX_P	E36	RST_SUP_B	V5	VSS
A15	AVSS_PCIE	E4	DDR_DQ11	V6	VDDIO_DDR
A16	VDD	E5	VDDIO_DDR	V7	VSS
A17	VDD	E6	VSS	W1	DDR_ADDR4
A19	MSH_DATA2	E7	VSS	W11	VSS
A2	VSS	E8	VSS	W12	VSS
A20	MSH_DATA7	E9	VSS	W13	VDD
A22	QSPI_DATA2	F1	VSS	W14	VSS
A23	TDI	F10	VSS	W15	VDD
A25	SCL_SOC0	F11	PCIE_REFCLK_P	W16	VSS
A26	SDA_SOC1	F12	AVSS_PCIE	W17	VDD
A28	MDIO_B0	F13	CORE_REFCLK_P	W18	VSS
A29	MDC_SOC	F14	VSS	W19	VDD
A3	DDR_DQ4	F15	PTP_REFCLK_P	W2	DDR_ADDR3
A31	GPIOHS15	F16	VDD	W20	VSS
A32	GPIOHS5	F17	VDD	W21	VDD
A34	GPIOHS8	F18	VDD	W22	VSS
A35	DEBUG_MODE0	F19	VSS	W23	VDD
A36	VSS	F2	VDDIO_DDR	W24	VSS
A37	VSS	F20	VSS	W25	VDD
A4	DDR_DM0	F21	VSS	W26	VDDOUT_G3
A5	VSS	F22	SD_WP	W27	VDDIO33
A6	HS_RX_P0	F23	VSS	W3	DDR_ADDR6
A7	VSS	F24	VSS	W31	VSS
A8	HS_RX_P1	F25	VSS	W32	HSS_REFCLK_P
A9	VSS	F26	MDC_A1	W33	HSS_REFCLK_N

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AA1	DDR_ADDR1	F27	VSS	W34	VSS
AA11	VDD_USB	F28	GPIO1	W35	VSS
AA12	VSS	F29	VSS	W36	HS_S0_REFCLK_N
AA13	VDD	F3	DDR_DQ14	W37	HS_S0_REFCLK_P
AA14	VSS	F30	GPIOHS10	W4	DDR_ADDR9
AA15	VDD	F31	VSS	W5	VSS
AA16	VSS	F32	DEBUG2	W6	VDDIO_DDR
AA17	VDD	F33	DEBUG_MODE2	W7	VSS
AA18	VSS	F34	DEBUG4	Y1	DDR_TEN
AA19	VDD	F35	CFG_PLL_SUP_BYP	Y11	AVDD33_USB
AA2	DDR_ADDR0	F36	UART_TXD0	Y12	VDD
AA20	VSS	F37	UART_RXD0	Y13	VSS
AA21	VDD	F4	DDR_DQ10	Y14	VDD
AA22	VSS	F5	VSS	Y15	VSS
AA23	VDD	F6	VSS	Y16	VDD
AA24	VSS	F7	VSS	Y17	VSS
AA25	VDD	F8	HS_CMU_REFCLK_P	Y18	VDD
AA26	VDDOUT_RECV	F9	VSS	Y19	VSS
AA27	VDDIO3318_RECV	G1	DDR_DQS_P1	Y2	DDR_BA0
AA3	DDR_ADDR5	G10	VSS	Y20	VDD
AA31	VSS	G11	PCIE_REFCLK_N	Y21	VSS
AA32	VSS	G12	AVSS_PCIE	Y22	VDD
AA33	CS_REFCLK_N	G13	CORE_REFCLK_N	Y23	VSS
AA34	CS_REFCLK_P	G14	VSS	Y24	VDD
AA35	VSS	G15	PTP_REFCLK_N	Y25	VSS
AA36	CS_S1_RX_N7	G16	VSS	Y26	VDDOUT_G4
AA37	CS_S1_RX_P7	G17	VDD	Y27	VDDIO33
AA4	DDR_ADDR8	G18	VDD	Y3	VSS
AA5	DDR_RST_B	G19	VDD	Y31	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AA6	VDDIO_DDR	G2	DDR_DQS_N1	Y32	VSS
AA7	VSS	G20	VSS	Y33	VSS
AB1	DDR_ADDR7	G21	VDDIO18_EFUSE_MEM	Y34	VSS
AB11	AVDD33_USB	G22	VDDIO18_EFUSE_INFO	Y35	VSS
AB12	VDD	G23	VSS	Y36	VSS
AB13	VSS	G24	VSS	Y37	VSS
AB14	VDD	G25	VSS	Y4	VDDIO_DDR
AB15	VSS	G26	VSS	Y5	DDR_PAR
AB16	VDD	G27	VSS	Y6	VDDIO_DDR
AB17	VSS	G28	VSS	Y7	VSS
AB18	VDD	G29	VSS	AL11	VSS
AB19	VSS	G3	DDR_DQ9	AL12	HS_S1_TX_P10
AB2	DDR_ADDR13	G30	VSS	AL13	VSS
AB20	VDD	G31	VSS	AL14	VSS
AB21	VSS	G32	VSS	AL15	VSS
AB22	AVDD18_CS	G33	TOD_REFCLK	AL16	VSS
AB23	AVDD18_CS	G34	CFG_PLL_CORE_BYP	AL17	VSS
AB24	AVDD18_CS	G35	UART_RXD2	AL18	VSS
AB25	AVDD18_CS	G36	UART_TXD1	AL19	HS_S1_TX_P15
AB26	AVDD18_CS	G37	UART_RXD1	AL2	HS_S0_RX_N2
AB27	AVDD18_CS	G4	DDR_DQ15	AL20	VSS
AB3	DDR_ADDR11	G5	VSS	AL21	VSS
AB31	CS_S1_TSTOUT	G6	VDDIO_DDR	AL22	HS_S2_TX_P17
AB32	VSS	G7	VSS	AL23	VSS
AB33	VSS	G8	HS_CMU_REFCLK_N	AL24	VSS
AB34	VSS	G9	VSS	AL25	HS_S2_TX_N19
AB35	VSS	H1	DDR_DQ18	AL26	VSS
AB36	VSS	H2	DDR_DM2	AL27	VSS
AB37	VSS	H3	DDR_DQ8	AL28	HS_S2_TX_P21

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AB4	DDR_ALERT_B	H31	VSS	AL29	VSS
AB5	DDR_ZQ	H32	BOOT_LPBK_TEST_MODE	AL3	VSS
AB6	VDDIO_DDR	H33	BOOT_USB_VREG_BYP	AL30	VSS
AB7	VSS	H34	BOOT_I2C_SA1	AL31	HS_S2_TX_N23
AC1	VSS	H35	VSS	AL32	VSS
AC11	VSS	H36	UART_TXD2	AL33	CS_S0_TX_P3
AC12	VSS	H4	VDDIO_DDR	AL34	CS_S0_TX_N3
AC13	VDD	H5	VSS	AL35	VSS
AC14	VSS	H6	VDDIO_DDR	AL36	CS_S0_RX_P0
AC15	VDD	H7	VSS	AL37	CS_S0_RX_N0
AC16	VSS	J1	DDR_DQ16	AL4	HS_S0_TX_N5
AC17	VDD	J2	DDR_DQ20	AL5	VSS
AC18	VSS	J3	DDR_DQ23	AL6	HS_S0_TX_P6
AC19	VDD	J31	VSS	AL7	VSS
AC2	VSS	J32	VSS	AL8	VSS
AC20	VSS	J33	BOOT_CPU_DIS	AL9	HS_S1_TX_N8
AC21	VDD	J34	BOOT_I2C_SA0	AM1	VSS
AC22	VSS	J35	BOOT_PCIE_RP_MODE	AM10	HS_S1_TX_N9
AC23	VSS	J36	BOOT_PCIE_FORCE_MODE	AM11	VSS
AC24	VSS	J37	BOOT_PCIE_AUTO_MODE	AM12	HS_S1_TX_N10
AC25	VSS	J4	DDR_DQ22	AM13	HS_S1_TX_P11
AC26	VSS	J5	VSS	AM14	VSS
AC27	VSS	J6	VDDIO_DDR	AM15	HS_S1_TX_N12
AC3	VSS	J7	VSS	AM16	VSS
AC31	VSS	K1	DDR_DQS_P2	AM17	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AC32	VSS	K11	HS_CMU_REXT10K	AM18	HS_S1_TX_N14
AC33	CS_S1_TX_P7	K12	AVDD09_VCO_HS3	AM19	HS_S1_TX_N15
AC34	CS_S1_TX_N7	K13	AVSS_PCIE	AM2	VSS
AC35	VSS	K14	AVSS_PCIE	AM20	VSS
AC36	CS_S1_RX_N5	K15	AVSS_PCIE	AM21	HS_S2_TX_P16
AC37	CS_S1_RX_P5	K16	AVDD18_THM	AM22	HS_S2_TX_N17
AC4	VSS	K17	VDD	AM23	VSS
AC5	USB_D_P	K18	VDD	AM24	HS_S2_TX_N18
AC6	USB_D_N	K19	AVDD18_DDRPLL	AM25	HS_S2_TX_P19
AC7	VSS	K2	DDR_DQS_N2	AM26	VSS
AD1	USB_TXR_TUNE	K20	VDD09_DDRPLL	AM27	HS_S2_TX_P20
AD11	VDD	K21	AVDD18_PLL	AM28	HS_S2_TX_N21
AD12	VDD	K22	AVDD18_LVDS	AM29	VSS
AD13	VSS	K23	VSS	AM3	VSS
AD14	VDD	K24	VSS	AM30	HS_S2_TX_N22
AD15	VSS	K25	VDDIO3318_MSH	AM31	HS_S2_TX_P23
AD16	VDD	K26	VDDIO3318_MSH	AM32	VSS
AD17	VSS	K27	VDDIO33	AM33	VSS
AD18	VDD	K3	DDR_DQ19	AM34	VSS
AD19	VSS	K31	VSS	AM35	VSS
AD2	USB_ID0	K32	BOOT_CPU_SPEED	AM36	VSS
AD20	VDD	K33	BOOT_STRAP0	AM37	VSS
AD21	VSS	K34	BOOT_RESV3	AM4	HS_S0_TX_P5
AD22	VDD	K35	BOOT_RESV1	AM5	VSS
AD23	VDD	K36	BOOT_RESV2	AM6	HS_S0_TX_N6
AD24	VDD	K37	BOOT_RESV0	AM7	HS_S0_TX_P7

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AD25	VDD	K4	DDR_DQ21	AM8	VSS
AD26	VDD	K5	VSS	AM9	HS_S1_TX_P8
AD27	VDD	K6	VDDIO_DDR	AN1	HS_S0_RX_P3
AD3	USB_VBUS0	K7	VSS	AN10	HS_S1_TX_P9
AD31	CS_S0_TSTOUT	L1	VSS	AN11	VSS
AD32	VSS	L11	VSS	AN12	VSS
AD33	VSS	L12	VSS	AN13	HS_S1_TX_N11
AD34	VSS	L13	AVSS_PCIE	AN14	VSS
AD35	VSS	L14	AVDD09_VCO_PCIE	AN15	HS_S1_TX_P12
AD36	VSS	L15	AVDD18_PCIE	AN16	HS_S1_TX_N13
AD37	VSS	L16	VSS	AN17	VSS
AD4	VSS	L17	VDD	AN18	HS_S1_TX_P14
AD5	VSS	L18	VDD	AN19	VSS
AD6	VSS	L19	AVSS_DDRPLL	AN2	HS_S0_RX_N3
AD7	VSS	L2	VDDIO_DDR	AN20	VSS
AE1	VSS	L20	VSS_DDRPLL	AN21	HS_S2_TX_N16
AE11	VSS	L21	AVSS_PLL	AN22	VSS
AE12	VSS	L22	VSS	AN23	VSS
AE13	VDD	L23	VDDOUT_MSH	AN24	HS_S2_TX_P18
AE14	VSS	L24	VDDOUT_G5	AN25	VSS
AE15	AVDD09_VCO_HS0	L25	VDDIO18	AN26	VSS
AE16	VSS	L26	VDDIO18	AN27	HS_S2_TX_N20
AE17	VDD	L27	VDDIO33	AN28	VSS
AE18	VSS	L3	DDR_DQ17	AN29	VSS
AE19	AVDD09_VCO_HS1	L31	VSS	AN3	VSS
AE2	VSS	L32	VSS	AN30	HS_S2_TX_P22
AE20	VSS	L33	BOOT_STRAP1	AN31	VSS
AE21	VDD	L34	BOOT_STRAP2	AN32	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AE22	VSS	L35	VSS	AN33	CS_S0_TX_P0
AE23	AVDD09_VCO_HS2	L36	BOOT_TEST_MODE	AN34	CS_S0_TX_N0
AE24	VSS	L4	VDDIO_DDR	AN35	VSS
AE25	VDD	L5	VSS	AN36	CS_S0_RX_P2
AE26	VSS	L6	VDDIO_DDR	AN37	CS_S0_RX_N2
AE27	VSS	L7	VSS	AN4	VSS
AE3	VSS	M1	DDR_CLK_N0	AN5	VSS
AE31	VSS	M11	AVDD18_HS3	AN6	VSS
AE32	VSS	M12	AVDD18_HS3	AN7	HS_S0_TX_N7
AE33	CS_S1_TX_N5	M13	AVDD18_HS3	AN8	VSS
AE34	CS_S1_TX_P5	M14	AVDD09_HS3	AN9	VSS
AE35	VSS	M15	AVSS_PCIE	AP1	VSS
AE36	CS_S1_RX_N6	M16	VDD	AP10	VSS
AE37	CS_S1_RX_P6	M17	VDD	AP11	VSS
AE4	VSS	M18	VDD	AP12	VSS
AE5	HS_S0_TX_P1	M19	VSS	AP13	VSS
AE6	HS_S0_TX_N1	M2	DDR_CLK_P0	AP14	VSS
AE7	VSS	M20	VDD	AP15	VSS
AF1	HS_S0_TX_N0	M21	VSS	AP16	HS_S1_TX_P13
AF11	AVDD09_HS0	M22	VDD	AP17	VSS
AF12	AVDD09_HS0	M23	VSS	AP18	VSS
AF13	AVDD09_HS0	M24	VDD	AP19	VSS
AF14	AVDD09_HS0	M25	VSS	AP2	VSS
AF15	VSS	M26	VDDOUT_MDIO_A	AP20	VSS
AF16	VSS	M27	VDDIO3312_MDIO_A	AP21	VSS
AF17	AVDD09_HS1	M3	DDR_ODT2	AP22	VSS
AF18	AVDD09_HS1	M31	VSS	AP23	VSS
AF19	VSS	M32	VSS	AP24	VSS
AF2	HS_S0_TX_P0	M33	GPIO9	AP25	VSS
AF20	AVDD09_HS1	M34	GPIO12	AP26	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AF21	AVDD09_HS1	M35	GPIO11	AP27	VSS
AF22	VSS	M36	GPIO10	AP28	VSS
AF23	VSS	M37	GPIO13	AP29	VSS
AF24	AVDD09_HS2	M4	DDR_CKE2	AP3	VSS
AF25	AVDD09_HS2	M5	DDR_CS_B3	AP30	VSS
AF26	AVDD09_HS2	M6	VDDIO_DDR	AP31	VSS
AF27	AVDD09_HS2	M7	VSS	AP32	VSS
AF3	VSS	N1	VSS	AP33	VSS
AF31	VSS	N11	VSS	AP34	VSS
AF32	VSS	N12	AVDD09_HS3	AP35	VSS
AF33	VSS	N13	AVDD09_HS3	AP36	VSS
AF34	VSS	N14	VSS	AP37	VSS
AF35	VSS	N15	AVDD09_PCIE	AP4	VSS
AF36	VSS	N16	VSS	AP5	VSS
AF37	VSS	N17	VDD	AP6	VSS
AF4	HS_S0_TX_N2	N18	VSS	AP7	VSS
AF5	HS_S0_TX_P2	N19	VDD	AP8	VSS
AF6	VSS	N2	VDDIO_DDR	AP9	VSS
AF7	VSS	N20	VSS	AR1	HS_S0_RX_N4
AG1	VSS	N21	VDD	AR10	VSS
AG11	HS_S0_CMU1_REXT10K	N22	VSS	AR11	HS_S1_RX_P10
AG12	VSS	N23	VDD	AR12	VSS
AG13	VSS	N24	VSS	AR13	VSS
AG14	VSS	N25	VDD	AR14	VSS
AG15	VSS	N26	VDDOUT_MDIO_B	AR15	VSS
AG16	VSS	N27	VDDIO3312_MDIO_B	AR16	VSS
AG17	VSS	N3	DDR_CS_B1	AR17	VSS
AG18	VSS	N31	VSS	AR18	VSS
AG19	AVDD18_HS1	N32	GPIO8	AR19	HS_S1_RX_P15
AG2	VSS	N33	LED_CLK	AR2	VSS
AG20	VSS	N34	LED_DATA	AR20	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AG21	VSS	N35	FUSE_DONE	AR21	VSS
AG22	VSS	N36	GPIO14	AR22	HS_S2_RX_N17
AG23	VSS	N37	GPIO15	AR23	VSS
AG24	VSS	N4	DDR_ODT0	AR24	VSS
AG25	VSS	N5	VSS	AR25	HS_S2_RX_N19
AG26	VSS	N6	VDDIO_DDR	AR26	VSS
AG27	HS_S2_CMU2_REXT10K	N7	VSS	AR27	VSS
AG3	VSS	P1	DDR_CLK_N1	AR28	HS_S2_RX_P21
AG31	VSS	P11	AVDD18_DATA_L16_DDR	AR29	VSS
AG32	VSS	P12	AVSS18_DATA_L16_DDR	AR3	VSS
AG33	CS_S1_TX_P6	P13	VDDIO_DDR	AR30	VSS
AG34	CS_S1_TX_N6	P14	VDD	AR31	HS_S2_RX_N23
AG35	VSS	P15	VSS	AR32	VSS
AG36	CS_S1_RX_P4	P16	VDD	AR33	CS_S0_TX_N2
AG37	CS_S1_RX_N4	P17	VSS	AR34	CS_S0_TX_P2
AG4	VSS	P18	VDD	AR35	VSS
AG5	VSS	P19	VSS	AR36	CS_S0_RX_P1
AG6	VSS	P2	DDR_CLK_P1	AR37	CS_S0_RX_N1
AG7	VSS	P20	VDD	AR4	VSS
AH1	HS_S0_RX_N0	P21	VSS	AR5	HS_S0_RX_P6
AH11	HS_S0_CMU2_REXT10K	P22	VDD	AR6	VSS
AH12	AVDD18_HS0	P23	VSS	AR7	VSS
AH13	AVDD18_HS0	P24	VDD	AR8	HS_S1_RX_N8
AH14	AVDD18_HS0	P25	VSS	AR9	VSS
AH15	AVDD18_HS0	P26	VDDIO18	AT1	HS_S0_RX_P4
AH16	HS_S1_CMU1_REXT10K	P27	VDDIO3318_GPIO_7_0	AT10	VSS
AH17	VSS	P3	DDR_CKE0	AT11	HS_S1_RX_N10

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AH18	AVDD18_HS1	P31	VSS	AT12	HS_S1_RX_P11
AH19	AVDD18_HS1	P32	VSS	AT13	VSS
AH2	HS_S0_RX_P0	P33	INTR_B1	AT14	HS_S1_RX_N12
AH20	AVDD18_HS1	P34	INTR_B0	AT15	VSS
AH21	VSS	P35	VSS	AT16	HS_S1_RX_N13
AH22	HS_S1_CMU2_REXT10K	P36	FUSE_FAIL	AT17	VSS
AH23	AVDD18_HS2	P4	DDR_ODT1	AT18	HS_S1_RX_N14
AH24	AVDD18_HS2	P5	VSS	AT19	HS_S1_RX_N15
AH25	AVDD18_HS2	P6	VDDIO_DDR	AT2	VSS
AH26	AVDD18_HS2	P7	VSS	AT20	VSS
AH27	HS_S2_CMU1_REXT10K	R1	DDR_CAS_B	AT21	HS_S2_RX_P16
AH3	VSS	R11	DDR_VREF1	AT22	HS_S2_RX_P17
AH31	VSS	R12	DDR_VREF0	AT23	VSS
AH32	VSS	R13	VDDIO_DDR	AT24	HS_S2_RX_N18
AH33	VSS	R14	VSS	AT25	HS_S2_RX_P19
AH34	VSS	R15	VDD	AT26	VSS
AH35	VSS	R16	VSS	AT27	HS_S2_RX_P20
AH36	VSS	R17	VDD	AT28	HS_S2_RX_N21
AH37	VSS	R18	VSS	AT29	VSS
AH4	VSS	R19	VDD	AT3	HS_S0_RX_N5
AH5	HS_S0_TX_P3	R2	DDR_ADDR14	AT30	HS_S2_RX_N22
AH6	HS_S0_TX_N3	R20	VSS	AT31	HS_S2_RX_P23
AH7	VSS	R21	VDD	AT32	VSS
AJ2	HS_S0_RX_N1	R22	VSS	AT33	VSS
AJ3	HS_S0_RX_P1	R23	VDD	AT34	VSS
AJ31	VSS	R24	VSS	AT35	VSS
AJ32	VSS	R25	VDD	AT36	VSS
AJ33	CS_S1_TX_P4	R26	VDDIO18	AT37	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
AJ34	CS_S1_TX_N4	R27	VDDOUT_GPIO_7_0	AT4	VSS
AJ35	VSS	R3	DDR_CS_B0	AT5	HS_S0_RX_N6
AJ36	CS_S0_RX_P3	R31	VSS	AT6	HS_S0_RX_P7
AJ37	CS_S0_RX_N3	R32	VSS	AT7	VSS
AJ4	VSS	R33	INTR_B2	AT8	HS_S1_RX_P8
AJ5	VSS	R34	INTR_B3	AT9	HS_S1_RX_N9
AJ6	HS_S0_TX_P4	R35	SYNC_CLK	AU1	VSS
AJ7	HS_S0_TX_N4	R36	SYNC_PULSE	AU10	VSS
AK1	VSS	R37	SYNC_CODE	AU12	HS_S1_RX_N11
AK2	VSS	R4	DDR_CKE1	AU13	VSS
AK3	VSS	R5	VSS	AU14	HS_S1_RX_P12
AK31	VSS	R6	VDDIO_DDR	AU15	VSS
AK32	VSS	R7	VSS	AU16	HS_S1_RX_P13
AK33	VSS	T1	DDR_RAS_B	AU17	VSS
AK34	VSS	T11	AVDD18_DATA_H8_DDR	AU18	HS_S1_RX_P14
AK35	VSS	T12	AVSS18_DATA_H8_DDR	AU2	VSS
AK36	VSS	T13	VDDIO_DDR	AU20	VSS
AK37	VSS	T14	VDD	AU21	HS_S2_RX_N16
AK4	VSS	T15	VSS	AU23	VSS
AK5	VSS	T16	VDD	AU24	HS_S2_RX_P18
AK6	VSS	T17	VSS	AU26	VSS
AK7	VSS	T18	VDD	AU27	HS_S2_RX_N20
AL1	HS_S0_RX_P2	T19	VSS	AU29	VSS
AL10	VSS	T2	DDR_WE_B	AU3	HS_S0_RX_P5
C32	GPIOHS3	T20	VDD	AU30	HS_S2_RX_P22
C33	VSS	T21	VSS	AU32	VSS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
C34	GPIOHS9	T22	VDD	AU33	CS_S0_TX_P1
C35	DEBUG5	T23	VSS	AU34	CS_S0_TX_N1
C36	WDT1_RST_B	T24	VDD	AU35	VSS
C37	WDT0_RST_B	T25	VSS	AU36	VSS
C4	DDR_DQ5	T26	VDDIO18	AU37	VSS
C5	VSS	T27	VDDIO33	AU4	VSS
C6	VSS	T3	DDR_CKE3	AU6	HS_S0_RX_N7
C7	HS_TX_P0	T31	VSS	AU7	VSS
C8	VSS	T32	TOD_PULSE	AU9	HS_S1_RX_P9
C9	HS_TX_P1	T33	TOD_CODE	B1	VSS
D1	DDR_DQ7	T34	RECV_CLK0	B10	VSS
D10	VSS	T35	VSS	B11	AVSS_PCIE
D11	AVSS_PCIE	T36	RECV_CLK1	B12	PCIE_TX_N
D12	AVSS_PCIE	T37	RECV_CLK2	B13	AVSS_PCIE
D13	PCIE_TPOUT	T4	DDR_CS_B2	B14	PCIE_RX_N
D14	PCIE_REXT	T5	VSS	B15	AVSS_PCIE
D15	VSS	T6	VDDIO_DDR	B16	VDD
D16	VDD	T7	VSS	B17	VDD
D17	VDD	U1	DDR_ADDR10	B18	THM_VINS0
D18	VSS	U11	VSS	B19	MSH_DATA1
D19	MSH_CMD	U12	VSS	B2	VDDIO_DDR
D2	DDR_DQ1	U13	VDDIO_DDR_CK	B20	MSH_DATA6
D20	MSH_DATA4	U14	VSS	B21	QSPI_DATA0
D21	QSPI_DATA1	U15	VDD	B22	QSPI_DATA3
D22	QSPI_CS0	U16	VSS	B23	TMS
D23	SD_SW_VOLT_EN	U17	VDD	B24	TDO

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
D24	MSCL0	U18	VSS	B25	SDA_SOC0
D25	MSDA1	U19	VDD	B26	SCL_SOC1
D26	MDIO_B1	U2	DDR_ADDR12	B27	MDIO_A0
D27	GPIO2	U20	VSS	B28	MDC_B0
D28	GPIO3	U21	VDD	B29	MDIO_SOC
D29	GPIO7	U22	VSS	B3	DDR_DQ3
D3	DDR_DQ0	U23	VDD	B30	GPIOHS1
D30	GPIOHS0	U24	VSS	B31	GPIOHS17
D31	GPIOHS12	U25	VDD	B32	GPIOHS4
D32	GPIOHS13	U26	VDDOUT_G1	B33	GPIOHS6
D33	GPIOHS2	U27	VDDIO33	B34	GPIOHS7
D34	DEBUG3	U3	VSS	B35	DEBUG6
D35	DEBUG7	U31	VSS	B36	DEBUG_MODE1
D36	USB_OVC_B	U32	VSS	B37	VSS
D37	CFG_GPIO_SEL	U33	VSS	B4	DDR_DQ6
D4	VDDIO_DDR	U34	VSS	B5	VSS
D5	VSS	U35	VSS	B6	HS_RX_N0
D6	VSS	U36	VSS	B7	VSS
D7	HS_TX_N0	U37	VSS	B8	HS_RX_N1
D8	VSS	U4	VDDIO_DDR	B9	VSS
D9	HS_TX_N1	U5	DDR_ODT3	C1	DDR_DQS_N0
E1	DDR_DM1	U6	VDDIO_DDR	C10	VSS
E10	VSS	U7	VSS	C11	AVSS_PCIE
E11	AVSS_PCIE	V1	DDR_BA2	C12	AVSS_PCIE
E12	AVSS_PCIE	V11	AVSS18_ADD_DDR	C13	AVSS_PCIE
E13	AVSS_PCIE	V12	AVDD18_ADD_DDR	C14	AVSS_PCIE
E14	VSS	V13	VDDIO_DDR	C15	VSS
E15	VSS	V14	VDD	C16	VDD
E16	VDD	V15	VSS	C17	VDD
E17	VDD	V16	VDD	C18	THM_VREFP

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
E18	VDD	V17	VSS	C19	MSH_DATA0
E19	MSH_CLK	V18	VDD	C2	DDR_DQS_P0
E2	DDR_DQ12	V19	VSS	C20	MSH_DATA5
E20	MSH_DATA3	V2	DDR_ADDR15	C21	VSS
E21	MSH_RST_B	V20	VDD	C22	QSPI_CLK
E22	QSPI_CS1	V21	VSS	C23	TCK
E23	SD_DET_B	V22	VDD	C24	VSS
E24	MSDA0	V23	VSS	C25	TRST_B
E25	MSCL1	V24	VDD	C26	MDC_A0
E26	MDIO_A1	V25	VSS	C27	VSS
E27	MDC_B1	V26	VDDOUT_G2	C28	GPIO5
E28	GPIO0	V27	VDDIO33	C29	GPIO4
E29	GPIO6	V3	DDR_BA1	C3	DDR_DQ2
E3	DDR_DQ13	V31	HS_S2_REFCLK_N	C30	VSS
E30	GPIOHS11	V32	HS_S2_REFCLK_P	C31	GPIOHS14

Table 7-8 : 5VT6126 Pin-Out Table (by Pin name)

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
AVDD18_ADD_DDR	V12	HS_TX_P0	C7	VSS	AH17
AVSS18_ADD_DDR	V11	HS_TX_P1	C9	VSS	AH21
AVDD18_PLL	K21	HSS_REFCLK_N	W33	VSS	AH3
AVDD18_DDRPLL	K19	HSS_REFCLK_P	W32	VSS	AH31
AVSS_PLL	L21	VDDIO18	L25	VSS	AH32
AVSS_DDRPLL	L19	VDDIO18	L26	VSS	AH33
BOOT_CPU_DIS	J33	INTR_B0	P34	VSS	AH34
BOOT_CPU_SPEED	K32	INTR_B1	P33	VSS	AH35
BOOT_I2C_SA0	J34	INTR_B2	R33	VSS	AH36
BOOT_I2C_SA1	H34	INTR_B3	R34	VSS	AH37
BOOT_LPBK_TEST_MODE	H32	LED_CLK	N33	VSS	AH4
BOOT_PCIE_AUTO_MODE	J37	LED_DATA	N34	VSS	AH7
BOOT_PCIE_FORCE_MODE	J36	MDC_A0	C26	VSS	AJ31

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
BOOT_PCIE_RP_MODE	J35	MDC_A1	F26	VSS	AJ32
BOOT_RESV0	K37	MDC_B0	B28	VSS	AJ35
BOOT_RESV1	K35	MDC_B1	E27	VSS	AJ4
BOOT_RESV2	K36	MDC_SOC	A29	VSS	AJ5
BOOT_RESV3	K34	MDIO_A0	B27	VSS	AK1
BOOT_STRAP0	K33	MDIO_A1	E26	VSS	AK2
BOOT_STRAP1	L33	MDIO_B0	A28	VSS	AK3
BOOT_STRAP2	L34	MDIO_B1	D26	VSS	AK31
BOOT_TEST_MODE	L36	MDIO_SOC	B29	VSS	AK32
BOOT_USB_VREG_BYP	H33	MSCL0	D24	VSS	AK33
CFG_GPIO_SEL	D37	MSCL1	E25	VSS	AK34
CFG_PLL_CORE_BYP	G34	MSDA0	E24	VSS	AK35
CFG_PLL_SUP_BYP	F35	MSDA1	D25	VSS	AK36
CORE_REFCLK_N	G13	MSH_CLK	E19	VSS	AK37
CORE_REFCLK_P	F13	MSH_CMD	D19	VSS	AK4
CS_REFCLK_N	AA33	MSH_DATA0	C19	VSS	AK5
CS_REFCLK_P	AA34	MSH_DATA1	B19	VSS	AK6
CS_S0_RX_N0	AL37	MSH_DATA2	A19	VSS	AK7
CS_S0_RX_N1	AR37	MSH_DATA3	E20	VSS	AL10
CS_S0_RX_N2	AN37	MSH_DATA4	D20	VSS	AL11
CS_S0_RX_N3	AJ37	MSH_DATA5	C20	VSS	AL13
CS_S0_RX_P0	AL36	MSH_DATA6	B20	VSS	AL14
CS_S0_RX_P1	AR36	MSH_DATA7	A20	VSS	AL15
CS_S0_RX_P2	AN36	MSH_RST_B	E21	VSS	AL16
CS_S0_RX_P3	AJ36	AVDD09_PCIE	N15	VSS	AL17
CS_S0_TSTOUT	AD31	AVDD09_VCO_PCIE	L14	VSS	AL18
CS_S0_TX_N0	AN34	AVDD18_PCIE	L15	VSS	AL20
CS_S0_TX_N1	AU34	AVSS_PCIE	A11	VSS	AL21
CS_S0_TX_N2	AR33	AVSS_PCIE	A13	VSS	AL23
CS_S0_TX_N3	AL34	AVSS_PCIE	A15	VSS	AL24
CS_S0_TX_P0	AN33	AVSS_PCIE	B11	VSS	AL26
CS_S0_TX_P1	AU33	AVSS_PCIE	B13	VSS	AL27

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
CS_S0_TX_P2	AR34	AVSS_PCIE	B15	VSS	AL29
CS_S0_TX_P3	AL33	AVSS_PCIE	C11	VSS	AL3
CS_S1_RX_N4	AG37	AVSS_PCIE	C12	VSS	AL30
CS_S1_RX_N5	AC36	AVSS_PCIE	C13	VSS	AL32
CS_S1_RX_N6	AE36	AVSS_PCIE	C14	VSS	AL35
CS_S1_RX_N7	AA36	AVSS_PCIE	D11	VSS	AL5
CS_S1_RX_P4	AG36	AVSS_PCIE	D12	VSS	AL7
CS_S1_RX_P5	AC37	AVSS_PCIE	E11	VSS	AL8
CS_S1_RX_P6	AE37	AVSS_PCIE	E12	VSS	AM1
CS_S1_RX_P7	AA37	AVSS_PCIE	E13	VSS	AM11
CS_S1_TSTOUT	AB31	AVSS_PCIE	F12	VSS	AM14
CS_S1_TX_N4	AJ34	AVSS_PCIE	G12	VSS	AM16
CS_S1_TX_N5	AE33	AVSS_PCIE	K13	VSS	AM17
CS_S1_TX_N6	AG34	AVSS_PCIE	K14	VSS	AM2
CS_S1_TX_N7	AC34	AVSS_PCIE	K15	VSS	AM20
CS_S1_TX_P4	AJ33	AVSS_PCIE	L13	VSS	AM23
CS_S1_TX_P5	AE34	AVSS_PCIE	M15	VSS	AM26
CS_S1_TX_P6	AG33	PCIE_REFCLK_N	G11	VSS	AM29
CS_S1_TX_P7	AC33	PCIE_REFCLK_P	F11	VSS	AM3
AVDD18_CS	AB22	PCIE_REXT	D14	VSS	AM32
AVDD18_CS	AB23	PCIE_RX_N	B14	VSS	AM33
AVDD18_CS	AB24	PCIE_RX_P	A14	VSS	AM34
AVDD18_CS	AB25	PCIE_TPOUT	D13	VSS	AM35
AVDD18_CS	AB26	PCIE_TX_N	B12	VSS	AM36
AVDD18_CS	AB27	PCIE_TX_P	A12	VSS	AM37
AVDD18_DATA_H8_DDR	T11	PTP_REFCLK_N	G15	VSS	AM5
AVSS18_DATA_H8_DDR	T12	PTP_REFCLK_P	F15	VSS	AM8
VDDIO_DDR_CK	U13	QSPI_CLK	C22	VSS	AN11
DDR_ADDR0	AA2	QSPI_CS0	D22	VSS	AN12
DDR_ADDR1	AA1	QSPI_CS1	E22	VSS	AN14
DDR_ADDR10	U1	QSPI_DATA0	B21	VSS	AN17
DDR_ADDR11	AB3	QSPI_DATA1	D21	VSS	AN19
DDR_ADDR12	U2	QSPI_DATA2	A22	VSS	AN20

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
DDR_ADDR13	AB2	QSPI_DATA3	B22	VSS	AN22
DDR_ADDR14	R2	RECV_CLK0	T34	VSS	AN23
DDR_ADDR15	V2	RECV_CLK1	T36	VSS	AN25
DDR_ADDR2	V4	RECV_CLK2	T37	VSS	AN26
DDR_ADDR3	W2	RST_SUP_B	E36	VSS	AN28
DDR_ADDR4	W1	SCL_SOC0	A25	VSS	AN29
DDR_ADDR5	AA3	SCL_SOC1	B26	VSS	AN3
DDR_ADDR6	W3	SD_DET_B	E23	VSS	AN31
DDR_ADDR7	AB1	SD_SW_VOLT_EN	D23	VSS	AN32
DDR_ADDR8	AA4	SD_WP	F22	VSS	AN35
DDR_ADDR9	W4	SDA_SOC0	B25	VSS	AN4
DDR_ALERT_B	AB4	SDA_SOC1	A26	VSS	AN5
DDR_BA0	Y2	AVDD18_DATA_L16_DDR	P11	VSS	AN6
DDR_BA1	V3	AVSS18_DATA_L16_DDR	P12	VSS	AN8
DDR_BA2	V1	SYNC_CLK	R35	VSS	AN9
DDR_CAS_B	R1	SYNC_CODE	R37	VSS	AP1
DDR_CKE0	P3	SYNC_PULSE	R36	VSS	AP10
DDR_CKE1	R4	TCK	C23	VSS	AP11
DDR_CKE2	M4	TDI	A23	VSS	AP12
DDR_CKE3	T3	TDO	B24	VSS	AP13
DDR_CLK_N0	M1	AVDD18_THM	K16	VSS	AP14
DDR_CLK_N1	P1	THM_VINS0	B18	VSS	AP15
DDR_CLK_P0	M2	THM_VREFP	C18	VSS	AP17
DDR_CLK_P1	P2	TMS	B23	VSS	AP18
DDR_CS_B0	R3	TOD_CODE	T33	VSS	AP19
DDR_CS_B1	N3	TOD_PULSE	T32	VSS	AP2
DDR_CS_B2	T4	TOD_REFCLK	G33	VSS	AP20
DDR_CS_B3	M5	TRST_B	C25	VSS	AP21
DDR_DM0	A4	UART_RXD0	F37	VSS	AP22
DDR_DM1	E1	UART_RXD1	G37	VSS	AP23

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
DDR_DM2	H2	UART_RXD2	G35	VSS	AP24
DDR_DQ0	D3	UART_TXD0	F36	VSS	AP25
DDR_DQ1	D2	UART_TXD1	G36	VSS	AP26
DDR_DQ10	F4	UART_TXD2	H36	VSS	AP27
DDR_DQ11	E4	USB_D_N	AC6	VSS	AP28
DDR_DQ12	E2	USB_D_P	AC5	VSS	AP29
DDR_DQ13	E3	VDD_USB	AA11	VSS	AP3
DDR_DQ14	F3	USB_ID0	AD2	VSS	AP30
DDR_DQ15	G4	USB_OVC_B	D36	VSS	AP31
DDR_DQ16	J1	USB_TXR_TUNE	AD1	VSS	AP32
DDR_DQ17	L3	USB_VBUS0	AD3	VSS	AP33
DDR_DQ18	H1	AVDD33_USB	Y11	VSS	AP34
DDR_DQ19	K3	AVDD33_USB	AB11	VSS	AP35
DDR_DQ2	C3	VDD	A16	VSS	AP36
DDR_DQ20	J2	VDD	A17	VSS	AP37
DDR_DQ21	K4	VDD	AA13	VSS	AP4
DDR_DQ22	J4	VDD	AA15	VSS	AP5
DDR_DQ23	J3	VDD	AA17	VSS	AP6
DDR_DQ3	B3	VDD	AA19	VSS	AP7
DDR_DQ4	A3	VDD	AA21	VSS	AP8
DDR_DQ5	C4	VDD	AA23	VSS	AP9
DDR_DQ6	B4	VDD	AA25	VSS	AR10
DDR_DQ7	D1	VDD	AB12	VSS	AR12
DDR_DQ8	H3	VDD	AB14	VSS	AR13
DDR_DQ9	G3	VDD	AB16	VSS	AR14
DDR_DQS_N0	C1	VDD	AB18	VSS	AR15
DDR_DQS_N1	G2	VDD	AB20	VSS	AR16
DDR_DQS_N2	K2	VDD	AC13	VSS	AR17
DDR_DQS_P0	C2	VDD	AC15	VSS	AR18
DDR_DQS_P1	G1	VDD	AC17	VSS	AR2
DDR_DQS_P2	K1	VDD	AC19	VSS	AR20
DDR_ODT0	N4	VDD	AC21	VSS	AR21
DDR_ODT1	P4	VDD	AD11	VSS	AR23
DDR_ODT2	M3	VDD	AD12	VSS	AR24
DDR_ODT3	U5	VDD	AD14	VSS	AR26

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
DDR_PAR	Y5	VDD	AD16	VSS	AR27
DDR_RAS_B	T1	VDD	AD18	VSS	AR29
DDR_RST_B	AA5	VDD	AD20	VSS	AR3
DDR_TEN	Y1	VDD	AD22	VSS	AR30
VDDIO_DDR	AA6	VDD	AD23	VSS	AR32
VDDIO_DDR	AB6	VDD	AD24	VSS	AR35
VDDIO_DDR	B2	VDD	AD25	VSS	AR4
VDDIO_DDR	D4	VDD	AD26	VSS	AR6
VDDIO_DDR	E5	VDD	AD27	VSS	AR7
VDDIO_DDR	F2	VDD	AE13	VSS	AR9
VDDIO_DDR	G6	VDD	AE17	VSS	AT10
VDDIO_DDR	H4	VDD	AE21	VSS	AT13
VDDIO_DDR	H6	VDD	AE25	VSS	AT15
VDDIO_DDR	J6	VDD	B16	VSS	AT17
VDDIO_DDR	K6	VDD	B17	VSS	AT2
VDDIO_DDR	L2	VDD	C16	VSS	AT20
VDDIO_DDR	L4	VDD	C17	VSS	AT23
VDDIO_DDR	L6	VDD	D16	VSS	AT26
VDDIO_DDR	M6	VDD	D17	VSS	AT29
VDDIO_DDR	N2	VDD	E16	VSS	AT32
VDDIO_DDR	N6	VDD	E17	VSS	AT33
VDDIO_DDR	P13	VDD	E18	VSS	AT34
VDDIO_DDR	P6	VDD	F16	VSS	AT35
VDDIO_DDR	R13	VDD	F17	VSS	AT36
VDDIO_DDR	R6	VDD	F18	VSS	AT37
VDDIO_DDR	T13	VDD	G17	VSS	AT4
VDDIO_DDR	T6	VDD	G18	VSS	AT7
VDDIO_DDR	U4	VDD	G19	VSS	AU1
VDDIO_DDR	U6	VDD	K17	VSS	AU10
VDDIO_DDR	V13	VDD	K18	VSS	AU13
VDDIO_DDR	V6	VDD	L17	VSS	AU15
VDDIO_DDR	W6	VDD	L18	VSS	AU17
VDDIO_DDR	Y4	VDD	M16	VSS	AU2
VDDIO_DDR	Y6	VDD	M17	VSS	AU20
DDR_VREF0	R12	VDD	M18	VSS	AU23
DDR_VREF1	R11	VDD	M20	VSS	AU26
DDR_WE_B	T2	VDD	M22	VSS	AU29

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
DDR_ZQ	AB5	VDD	M24	VSS	AU32
DEBUG_MODE0	A35	VDD	N17	VSS	AU35
DEBUG_MODE1	B36	VDD	N19	VSS	AU36
DEBUG_MODE2	F33	VDD	N21	VSS	AU37
DEBUG0	E33	VDD	N23	VSS	AU4
DEBUG1	E34	VDD	N25	VSS	AU7
DEBUG2	F32	VDD	P14	VSS	B1
DEBUG3	D34	VDD	P16	VSS	B10
DEBUG4	F34	VDD	P18	VSS	B37
DEBUG5	C35	VDD	P20	VSS	B5
DEBUG6	B35	VDD	P22	VSS	B7
DEBUG7	D35	VDD	P24	VSS	B9
VDDIO18_EFUSE_INFO	G22	VDD	R15	VSS	C10
VDDIO18_EFUSE_MEM	G21	VDD	R17	VSS	C15
FUSE_DONE	N35	VDD	R19	VSS	C21
FUSE_FAIL	P36	VDD	R21	VSS	C24
GPIO0	E28	VDD	R23	VSS	C27
GPIO1	F28	VDD	R25	VSS	C30
GPIO10	M36	VDD	T14	VSS	C33
GPIO11	M35	VDD	T16	VSS	C5
GPIO12	M34	VDD	T18	VSS	C6
GPIO13	M37	VDD	T20	VSS	C8
GPIO14	N36	VDD	T22	VSS	D10
GPIO15	N37	VDD	T24	VSS	D15
GPIO2	D27	VDD	U15	VSS	D18
GPIO3	D28	VDD	U17	VSS	D5
GPIO4	C29	VDD	U19	VSS	D6
GPIO5	C28	VDD	U21	VSS	D8
GPIO6	E29	VDD	U23	VSS	E10
GPIO7	D29	VDD	U25	VSS	E14
GPIO8	N32	VDD	V14	VSS	E15
GPIO9	M33	VDD	V16	VSS	E32
GPIOHS0	D30	VDD	V18	VSS	E35
GPIOHS1	B30	VDD	V20	VSS	E6
GPIOHS10	F30	VDD	V22	VSS	E7
GPIOHS11	E30	VDD	V24	VSS	E8
GPIOHS12	D31	VDD	W13	VSS	E9

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
GPIOHS13	D32	VDD	W15	VSS	F1
GPIOHS14	C31	VDD	W17	VSS	F10
GPIOHS15	A31	VDD	W19	VSS	F14
GPIOHS16	E31	VDD	W21	VSS	F19
GPIOHS17	B31	VDD	W23	VSS	F20
GPIOHS2	D33	VDD	W25	VSS	F21
GPIOHS3	C32	VDD	Y12	VSS	F23
GPIOHS4	B32	VDD	Y14	VSS	F24
GPIOHS5	A32	VDD	Y16	VSS	F25
GPIOHS6	B33	VDD	Y18	VSS	F27
GPIOHS7	B34	VDD	Y20	VSS	F29
GPIOHS8	A34	VDD	Y22	VSS	F31
GPIOHS9	C34	VDD	Y24	VSS	F5
HS_CMU_REFCLK_N	G8	VDD09_DDRPLL	K20	VSS	F6
HS_CMU_REFCLK_P	F8	AVDD18_LVDS	K22	VSS	F7
HS_CMU_REXT10K	K11	VDDIO18	T26	VSS	F9
HS_RX_N0	B6	VDDOUT_GPIO_7_0	R27	VSS	G10
HS_RX_N1	B8	VDDIO18	P26	VSS	G14
HS_RX_P0	A6	VDDIO18	R26	VSS	G16
HS_RX_P1	A8	VDDOUT_MDIO_A	M26	VSS	G20
AVDD09_HS0	AF11	VDDOUT_MDIO_B	N26	VSS	G23
AVDD09_HS0	AF12	VDDOUT_MSH	L23	VSS	G24
AVDD09_HS0	AF13	VDDOUT_RECV	AA26	VSS	G25
AVDD09_HS0	AF14	VDDOUT_G1	U26	VSS	G26
AVDD09_VCO_HS0	AE15	VDDOUT_G2	V26	VSS	G27
AVDD18_HS0	AH12	VDDOUT_G3	W26	VSS	G28
AVDD18_HS0	AH13	VDDOUT_G4	Y26	VSS	G29
AVDD18_HS0	AH14	VDDOUT_G5	L24	VSS	G30
AVDD18_HS0	AH15	VDDIO33	K27	VSS	G31
HS_S0_CMU1_REXT10K	AG11	VDDIO33	L27	VSS	G32

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
HS_S0_CMU2_REXT10K	AH11	VDDIO33	T27	VSS	G5
HS_S0_REFCLK_N	W36	VDDIO33	U27	VSS	G7
HS_S0_REFCLK_P	W37	VDDIO33	V27	VSS	G9
HS_S0_RX_N0	AH1	VDDIO33	W27	VSS	H31
HS_S0_RX_N1	AJ2	VDDIO33	Y27	VSS	H35
HS_S0_RX_N2	AL2	VDDIO3318_GPIO_7_0	P27	VSS	H5
HS_S0_RX_N3	AN2	VDDIO3312_MDIO_A	M27	VSS	H7
HS_S0_RX_N4	AR1	VDDIO3312_MDIO_B	N27	VSS	J31
HS_S0_RX_N5	AT3	VDDIO3318_MSH	K25	VSS	J32
HS_S0_RX_N6	AT5	VDDIO3318_MSH	K26	VSS	J5
HS_S0_RX_N7	AU6	VDDIO3318_RECV	AA27	VSS	J7
HS_S0_RX_P0	AH2	VSS	A1	VSS	K23
HS_S0_RX_P1	AJ3	VSS	A10	VSS	K24
HS_S0_RX_P2	AL1	VSS	A2	VSS	K31
HS_S0_RX_P3	AN1	VSS	A36	VSS	K5
HS_S0_RX_P4	AT1	VSS	A37	VSS	K7
HS_S0_RX_P5	AU3	VSS	A5	VSS	L1
HS_S0_RX_P6	AR5	VSS	A7	VSS	L11
HS_S0_RX_P7	AT6	VSS	A9	VSS	L12
HS_S0_TX_N0	AF1	VSS	AA12	VSS	L16
HS_S0_TX_N1	AE6	VSS	AA14	VSS	L22
HS_S0_TX_N2	AF4	VSS	AA16	VSS	L31
HS_S0_TX_N3	AH6	VSS	AA18	VSS	L32
HS_S0_TX_N4	AJ7	VSS	AA20	VSS	L35
HS_S0_TX_N5	AL4	VSS	AA22	VSS	L5
HS_S0_TX_N6	AM6	VSS	AA24	VSS	L7
HS_S0_TX_N7	AN7	VSS	AA31	VSS	M19
HS_S0_TX_P0	AF2	VSS	AA32	VSS	M21
HS_S0_TX_P1	AE5	VSS	AA35	VSS	M23
HS_S0_TX_P2	AF5	VSS	AA7	VSS	M25
HS_S0_TX_P3	AH5	VSS	AB13	VSS	M31
HS_S0_TX_P4	AJ6	VSS	AB15	VSS	M32
HS_S0_TX_P5	AM4	VSS	AB17	VSS	M7
HS_S0_TX_P6	AL6	VSS	AB19	VSS	N1

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
HS_S0_TX_P7	AM7	VSS	AB21	VSS	N11
AVDD09_HS1	AF17	VSS	AB32	VSS	N14
AVDD09_HS1	AF18	VSS	AB33	VSS	N16
AVDD09_HS1	AF20	VSS	AB34	VSS	N18
AVDD09_HS1	AF21	VSS	AB35	VSS	N20
AVDD09_VCO_HS1	AE19	VSS	AB36	VSS	N22
AVDD18_HS1	AG19	VSS	AB37	VSS	N24
AVDD18_HS1	AH18	VSS	AB7	VSS	N31
AVDD18_HS1	AH19	VSS	AC1	VSS	N5
AVDD18_HS1	AH20	VSS	AC11	VSS	N7
HS_S1_CMU1_REXT10K	AH16	VSS	AC12	VSS	P15
HS_S1_CMU2_REXT10K	AH22	VSS	AC14	VSS	P17
HS_S1_REFCLK_N	V35	VSS	AC16	VSS	P19
HS_S1_REFCLK_P	V36	VSS	AC18	VSS	P21
HS_S1_RX_N10	AT11	VSS	AC2	VSS	P23
HS_S1_RX_N11	AU12	VSS	AC20	VSS	P25
HS_S1_RX_N12	AT14	VSS	AC22	VSS	P31
HS_S1_RX_N13	AT16	VSS	AC23	VSS	P32
HS_S1_RX_N14	AT18	VSS	AC24	VSS	P35
HS_S1_RX_N15	AT19	VSS	AC25	VSS	P5
HS_S1_RX_N8	AR8	VSS	AC26	VSS	P7
HS_S1_RX_N9	AT9	VSS	AC27	VSS	R14
HS_S1_RX_P10	AR11	VSS	AC3	VSS	R16
HS_S1_RX_P11	AT12	VSS	AC31	VSS	R18
HS_S1_RX_P12	AU14	VSS	AC32	VSS	R20
HS_S1_RX_P13	AU16	VSS	AC35	VSS	R22
HS_S1_RX_P14	AU18	VSS	AC4	VSS	R24
HS_S1_RX_P15	AR19	VSS	AC7	VSS	R31
HS_S1_RX_P8	AT8	VSS	AD13	VSS	R32
HS_S1_RX_P9	AU9	VSS	AD15	VSS	R5
HS_S1_TX_N10	AM12	VSS	AD17	VSS	R7
HS_S1_TX_N11	AN13	VSS	AD19	VSS	T15
HS_S1_TX_N12	AM15	VSS	AD21	VSS	T17
HS_S1_TX_N13	AN16	VSS	AD32	VSS	T19
HS_S1_TX_N14	AM18	VSS	AD33	VSS	T21
HS_S1_TX_N15	AM19	VSS	AD34	VSS	T23
HS_S1_TX_N8	AL9	VSS	AD35	VSS	T25

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
HS_S1_TX_N9	AM10	VSS	AD36	VSS	T31
HS_S1_TX_P10	AL12	VSS	AD37	VSS	T35
HS_S1_TX_P11	AM13	VSS	AD4	VSS	T5
HS_S1_TX_P12	AN15	VSS	AD5	VSS	T7
HS_S1_TX_P13	AP16	VSS	AD6	VSS	U11
HS_S1_TX_P14	AN18	VSS	AD7	VSS	U12
HS_S1_TX_P15	AL19	VSS	AE1	VSS	U14
HS_S1_TX_P8	AM9	VSS	AE11	VSS	U16
HS_S1_TX_P9	AN10	VSS	AE12	VSS	U18
AVDD09_HS2	AF24	VSS	AE14	VSS	U20
AVDD09_HS2	AF25	VSS	AE16	VSS	U22
AVDD09_HS2	AF26	VSS	AE18	VSS	U24
AVDD09_HS2	AF27	VSS	AE2	VSS	U3
AVDD09_VCO_HS2	AE23	VSS	AE20	VSS	U31
AVDD18_HS2	AH23	VSS	AE22	VSS	U32
AVDD18_HS2	AH24	VSS	AE24	VSS	U33
AVDD18_HS2	AH25	VSS	AE26	VSS	U34
AVDD18_HS2	AH26	VSS	AE27	VSS	U35
HS_S2_CMU1_REXT10K	AH27	VSS	AE3	VSS	U36
HS_S2_CMU2_REXT10K	AG27	VSS	AE31	VSS	U37
HS_S2_REFCLK_N	V31	VSS	AE32	VSS	U7
HS_S2_REFCLK_P	V32	VSS	AE35	VSS	V15
HS_S2_RX_N16	AU21	VSS	AE4	VSS	V17
HS_S2_RX_N17	AR22	VSS	AE7	VSS	V19
HS_S2_RX_N18	AT24	VSS	AF15	VSS	V21
HS_S2_RX_N19	AR25	VSS	AF16	VSS	V23
HS_S2_RX_N20	AU27	VSS	AF19	VSS	V25
HS_S2_RX_N21	AT28	VSS	AF22	VSS	V33
HS_S2_RX_N22	AT30	VSS	AF23	VSS	V34
HS_S2_RX_N23	AR31	VSS	AF3	VSS	V5
HS_S2_RX_P16	AT21	VSS	AF31	VSS	V7
HS_S2_RX_P17	AT22	VSS	AF32	VSS	W11
HS_S2_RX_P18	AU24	VSS	AF33	VSS	W12
HS_S2_RX_P19	AT25	VSS	AF34	VSS	W14
HS_S2_RX_P20	AT27	VSS	AF35	VSS	W16
HS_S2_RX_P21	AR28	VSS	AF36	VSS	W18
HS_S2_RX_P22	AU30	VSS	AF37	VSS	W20

Pin Name	Ball	Pin Name	Ball	Pin Name	Ball
HS_S2_RX_P23	AT31	VSS	AF6	VSS	W22
HS_S2_TX_N16	AN21	VSS	AF7	VSS	W24
HS_S2_TX_N17	AM22	VSS	AG1	VSS	W31
HS_S2_TX_N18	AM24	VSS	AG12	VSS	W34
HS_S2_TX_N19	AL25	VSS	AG13	VSS	W35
HS_S2_TX_N20	AN27	VSS	AG14	VSS	W5
HS_S2_TX_N21	AM28	VSS	AG15	VSS	W7
HS_S2_TX_N22	AM30	VSS	AG16	VSS	Y13
HS_S2_TX_N23	AL31	VSS	AG17	VSS	Y15
HS_S2_TX_P16	AM21	VSS	AG18	VSS	Y17
HS_S2_TX_P17	AL22	VSS	AG2	VSS	Y19
HS_S2_TX_P18	AN24	VSS	AG20	VSS	Y21
HS_S2_TX_P19	AM25	VSS	AG21	VSS	Y23
HS_S2_TX_P20	AM27	VSS	AG22	VSS	Y25
HS_S2_TX_P21	AL28	VSS	AG23	VSS	Y3
HS_S2_TX_P22	AN30	VSS	AG24	VSS	Y31
HS_S2_TX_P23	AM31	VSS	AG25	VSS	Y32
AVDD09_HS3	M14	VSS	AG26	VSS	Y33
AVDD09_HS3	N12	VSS	AG3	VSS	Y34
AVDD09_HS3	N13	VSS	AG31	VSS	Y35
AVDD09_VCO_HS3	K12	VSS	AG32	VSS	Y36
AVDD18_HS3	M11	VSS	AG35	VSS	Y37
AVDD18_HS3	M12	VSS	AG4	VSS	Y7
AVDD18_HS3	M13	VSS	AG5	VSS_DDRPLL	L20
HS_TX_N0	D7	VSS	AG6	WDT0_RST_B	C37
HS_TX_N1	D9	VSS	AG7	WDT1_RST_B	C36

8 Pin Information

8.1 Pin information –Grouped by function

Note[1]: PU/PD is internal Pull Up or Pull Down of LVCMOS IO, the internal pull-up resistor ranges from 33 kΩ to 88K kΩ (typical value is 58K kΩ) while the internal pull-down resistor ranges from 34K kΩ to 93 kΩ (typical value is 60K kΩ)

Note[2]: If not indicate specifically, LVCMOS is 3.3V (typ) IO

Note[3]: “I”/”O”/”B” in Type column represent “Input”/”Output”/”Bi-Direction” respectively.

Note[4]: “OD” is open-drain IO, external pull-up resistor should be used.

Note[5]: DDR SSTL-15 voltage 1.35V(DDR3L) or 1.5V(DDR3), 1.2V(DDR4) SSTL and POD can be selected via configuring on die termination.

Note[6]: Support 1.8V/3.3V I/O, if the frequency exceeds 50MHz, it is recommended to use 1.8 I/O, for 0~50Mhz frequency, 1.8 /3.3V can be used.

Note[7]: The pull up or pull down are only effective for those input PAD or bi-directional PAD while used as input.

Table 8-1 : Pin information –Function Signals

Pin Name	Type	Rate	Pin #	PU/ PD	Description
Octal SerDes (HSS12G) Interface					
HS_S[0:2]_REFCLK_P HS_S[0:2]_REFCLK_N	I LVDS	156.25MHz	6	-	HSS12G input differential clock, impedance 100±10% Ohm.
HS_S[0:2]_REXT10k[1:2]	O LVCMOS	static	6	-	Reserve Pins. Should connect to via or keep floating.
HS_S[0:2]_RX_P[7:0] HS_S[0:2]_RX_N[7:0]	I CML IN	1.25G~12.5Gbps	48	-	1.25G~12.5Gbps SerDes links input. Typical configurations are: • 100Base-FX • SGMII,1.25Gbps • XAUI/10GBASE-KX4, 3.125Gbps • QSGMII,5Gbps • Usxgmii-Multiport,5.15625Gbps

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					• XFI/SFI/10GBASE-KR/USXGMII-Multiport, 10.3125Gbps • DXAUI,6.25Gbps • XLAUI/40GBASE-KR4/CR4, 10.3125Gbps
HS_S[0:2]_TX_P[7:0] HS_S[0:2]_TX_N[7:0]	O CML OUT	1.25G~12.5Gbps	48	-	1.25G~12.5Gbps SerDes links output.
SerDes (HSS28G) Interface					
CS_REFCLK_N CS_REFCLK_P	I LVDS	156.25MHz	2	-	28G SerDes input differential clock, impedance 100±10% Ohm.
HSS_REFCLK_P HSS_REFCLK_N	I LVDS	156.25MHz	2	-	Ext reference clock to generate sup clock used for: • PCS transmit clock for28G SerDes • Super clock for core digitallogic
CS_S[0:1]_RX[0:3]_P CS_S[0:1]_RX[0:3]_N	I CML IN	1.25G~28.125Gbps	16	-	1.25G~28Gbps SerDes links input Typical configurations are: • SGMII,1.25Gbps • XAUI/10GBASE-KX4, 3.125Gbps • QSGMII,5Gbps • Usxgmii-Multiport,5.15625Gbps • XFI/SFI/10GBASE-KR/USXGMII-Multiport, 10.3125Gbps • DXAUI,6.25Gbps • XLAUI/40GBASE-KR4/CR4, 10.3125Gbps • CAUI-4/100GBASE-KR4/CR4, 25.78125Gbps • 25GAUI/25GBASE-KR/CR, 25.78125Gbps • 50GBASE-CR2/KR2, 25.78125Gbps
CS_S[0:1]_TX[0:3]_P CS_S[0:1]_TX[0:3]_N	O CML OUT	1.25G~28.125Gbps	16	-	1.25G~28Gbps SerDes links output
CS_S[0:1]_TSTOUT	O Analog	Static	2	-	Analog output test pin, reserved for factory debug. Should connect to a via or keep floating.
PCIE SerDes (HSS5G) Interface					

Pin Name	Type	Rate	Pin #	PU/ PD	Description
PCIE_REFCLK_P PCIE_REFCLK_N	I HCSL	100MHz	2	-	PCIE input deferential reference clock 100M.
PCIE_RX_P PCIE_RX_N	I CML IN	2.5G/5Gbps	2	-	PCIE input data.
PCIE_TX_P PCIE_TX_N	O CML OUT	2.5G/5Gbps	2	-	PCIE output data.
PCIE_REXT	I LVCMOS	Static	1	-	External resistor for termination calibration: Connect 50 ohm external resistor (1% precision) between PCIE_REXT to AVDD18_PCIE (no need to be close to BGA BALL)
PCIE_TPOUT	O LVCMOS	static	1	-	Analog output test pin, reserved for factory debug. Should connect to a via.
Configuration					
RST_SUP_B	I LVCMOS	Static	1	PD	Global reset for chip, schmitter trigger. Active low.
CFG_GPIO_SEL	I LVCMOS	Static	1	PU	1'b1: GPIOHS[17:0] set to GPIO mode 1'b0: GPIOHS[17:0] set to TRACE debug mode
CFG_PLL_CORE_BYP	I LVCMOS	static	1	PD	If set, the internal PLL CORE will be bypassed, should tie to GND while bring up
CFG_PLL_SUP_BYP	I LVCMOS	static	1	PD	If set, the internal PLL SUP will be bypassed, should tie to GND while bring up
Configuration					
BOOT_PCIE_AUTO_MODE	I LVCMOS	-	1	PU	Define the Reset Mode of PCIE: 1’b1: De-assert the related reset signals of PCIe automatically 1’b0: user needs to de-assert the related reset signal manually by I²CSlave Interface(Debug Only)
BOOT_PCIE_FORCE_MODE	I LVCMOS	-	1	PU	Define the PCIE Mode: 1’b1: Force to operate at GEN1 Mode; 1’b0: Normal Mode
BOOT_PCIE_RP_MODE	I LVCMOS	-	1	PU	Tie to 3.3v if PCIe interface runs on Rootport mode.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					Otherwise, tie to GND
BOOT_STRAP[2:0]	I LVCMOS	-	3	PD	Define the internal CPU boot up mode: 3'b000: ROM + QSPI 3'b001: Reserved 3'b011: ROM + UART 3'b100: QSPI 3'b101: JTAG 3'b11x: Reserved
BOOT_CPU_SPEED	I LVCMOS	-	1	PU	0: Internal CPU runs1.2GHz 1: Internal CPU runs800MHz
BOOT_CPU_DIS	I LVCMOS	-	1	PD	0: Enable internal CPU 1: Disable internal CPU, PCIe interface must be brought up for this mode.
BOOT_TEST_MODE	I LVCMOS	-	1	PD	0: Function mode 1: Internal DFT Test mode CPU coresight JTAG should beunder function mode. Tie to GND
BOOT_I2C_SA[1:0]	I LVCMOS	-	2	PD	I^2C Slave address LSB2bits 7'b11_11xx (xx = 00 to11)
BOOT_RESV[3:0]	I LVCMOS	-	4	PU	All connect to 3.3V
BOOT_LPBK_TEST_MODE	I LVCMOS	-	1	PD	0: Function mode 1: Set to Interface IP loopback test mode Tie to GND
GPIO Interface					
GPIO[7:0]	B LVCMOS 1.8V/3.3V	0-150MHz/0-50MHz	8	-	General purpose IO GPIO[1:0]: also used in TsEngine **SysGpioMultiCtl**.*cfgGpio[N]Sel[1:0]* N=0..7, each field control the selection of each bit of GPIO[7:0] to be used as GPIO or SPI or FAN. 2'b00: GPIO => GPIO[7:0] 2'b01: SPI =>Bit0: SPI_CLK Bit1: SPI_FSS (could don't care)Bit2:SPI_MISO Bit3:SPI_MOSI

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					Bit[4:7]: SPI_CS_B[0:3] 2'b10: FAN => Bit[0:3]: TACH[0:3] FANs' status Bit[4:7]: PWM[0:3] control the FANs
GPIO[15:8]	B LVCMOS 3.3V	0-50MHz	8	-	General purpose IO **SysGpioMultiCtl**.*cfgGpio[N]Sel[1:0]* N=8..15, each field control the selection of each bit of GPIO[15:8] to be used as GPIO or UART or FAN. 2'b00: GPIO => GPIO[15:8] 2'b01: UART2 =>Bit10: UART2_DTR_NBit11: UART2_RTS_NBit12: UART2_CTS_NBit13: UART2_DSR_NBit14: UART2_DCD_NBit15: UART2_RI_N 2'b10: FAN => Bit[0:3]: PWM[0:3] control the FANs Bit[4:7]: TACH[0:3] FANs' status
GPIOHS[17:0]	B LVCMOS 1.8V	0~150MHz	18	-	CFG_GPIO_SEL: 0: used as DS-5 trace interfaceBit[0:15]: TRACE_DATA[0:15]Bit16:TRACE_CLK Bit17:TRACE_CTL 1: used as general purpose IO and OobFC **SysGpioHsMultiCtl**.*cfgGpioHs[N]Sel[1:0]* N=0..17,eachfieldcontrolthe selection of each bit of GIPIOHS[17:0]. 2'b00: used as GPIO 2'b01: used as OobFC: Bit0:FCIN_CLK Bit[1:2]: FCIN_DATA[0:1] Bit3: FCIN_SYNC Bit4: FCOUT_CLK Bit[5:6]: FCOUT_DATA[0:1]

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					Bit7: FCOUT_SYNC
MSH					
MSH_CMD	B LVCMOS 1.8V/3.3V	0-150MHz/0-50MHz	1	-	Bidirectional Commandchannel used for command and response transfers.
MSH_CLK	O LVCMOS 1.8V/3.3V	0-150MHz/0-50MHz	1	-	Output MSH CLK, always valid While the MSH IO power supply is 1.8V, the CLK frequency could be 0-150MHz, otherwise the CLK frequency is 0-50MHz.
MSH_DATA[7:0]	BLVCMOS 1.8V/3.3V	0-150MHz/0-50MHz	8	-	Bidirectional data signals.
MSH_RST_B	O LVCMOS 1.8V/3.3V	0-150MHz/0-50MHz	1	-	Reset the device and make the device to the pre-idle state. Active low. Only used for eMMC device.
SD_DET_B	I LVCMOS	0-50MHz	1	-	pull down with 1K ohm..
SD_WP	I LVCMOS	0-50MHz	1	-	pull down with 1K ohm.
SD_SW_VOLT_EN	-	-	-	-	Reserved
QSPI					
QSPI_CLK	O LVCMOS	50MHz	1	-	QSPI output clock
QSPI_CS[1:0]	O LVCMOS	Static	2	-	Chip Selection signal of QSPI interface
QSPI_DATA[3:0]	B LVCMOS	50MHz	4	-	QSPI bidirectional data
UART Interface					
UART_TXD[2:0]	O LVCMOS	5MHz	3	-	Tx Data of UART interface
UART_RXD[2:0]	I LVCMOS	5MHz	3	PD	Rx Data of UART interface
DDR SDRAM Interface					
DDR_CLK_P[1:0] DDR_CLK_N[1:0]	O SSTL	DDR3: 800MHz DDR4: 800MHz	4	-	Differential clock output
DDR_CKE[3:0]	O SSTL	See above	4	-	Clock enable, active high
DDR_CS_B[3:0]	O SSTL	See above	4	-	Chip select, Active low. Ensure each group signals are connected correctly. (For example, ODT0/CKE0/CS0) If only use one chip select pin, it must use DDR_CS_B0/ ODT0/ CKE0. And use two chip select pin, it must use DDR_CS_B0/B1.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
DDR_ODT[3:0]	O SSTL	See above	4	-	On-die termination
DDR_ADDR[15:0]	O SSTL	See above	16	-	Address output DDR_ADDR[14] is used as DDR_ACT_B of DDR4; DDR_ADDR[15] is used as DDR_BG[1] of DDR4.
DDR_BA[2:0]	O SSTL	See above	3	-	Bank addressoutput DDR_BA[2] is used as DDR_BG[0] ofDDR4.
DDR_RAS_B	O SSTL	See above	1	-	RAS command, active low Used as DDR4 DDR_ADDR[16] when DDR_ACT_B is low
DDR_CAS_B	O SSTL	See above	1	-	CAS command, active low Used as DDR4 DDR_ADDR[15] when DDR_ACT_B is low
DDR_WE_B	O SSTL	See above	1	-	WE command, active low Used as DDR4 DDR_ADDR[14] when DDR_ACT_B is low
DDR_RST_B	O SSTL	See above	1	-	Reset device, active low
DDR_DQ[23:0]	B SSTL	See above	24	-	DQ[15:0] used for pure data DQ[23:16] used for ECC, can NOT be used for data even ECC is disabled.
DDR_DQS_P[2:0] DDR_DQS_N[2:0]	B SSTL	See above	6	-	Data strobe Bit2: used for DDR_DQ[23:16] Bit1: used for DDR_DQ[15:8] Bit0: used for DDR_DQ[7:0]
DDR_DM[2:0]	O SSTL	See above	3	-	Data mask Bit2: used for DDR_DQ[23:16] Bit1: used for DDR_DQ[15:8] Bit0: used for DDR_DQ[7:0]
DDR_ZQ	B SSTL	See above	1	-	Calibration resistor for PVT compensation Should connect to external resistor 240 ohm (+/-1%)
DDR_PAR	O SSTL	See above	1	-	DDR4 command and address parity check
DDR_TEN	O SSTL	See above	1	-	DDR4 SDRAM connectivity test mode enable
DDR_ALERT_B	B SSTL	See above	1	-	DDR4 SDRAM used only: Input pin: DDR4 used for CRC and command/ address parity check. Active low.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					Ouput pin: connectivity test
DDR_VREF0	I PWR	-	1	-	Used for ATE IO DC test. Keep floating when application.
DDR_VREF1	I PWR	-	1	-	Used for ATE IO DC test. Keep floating when application.
USB					
USB_D_P	B Analog	480Mbps	1	-	USB D+ signal In HS operation, this pin receives/transmits a maximum of 800 mV or 400 mV nominally. In FS or LS operation, this pin receives/transmits 3.3V nominally.
USB_D_M	B Analog	480Mbps	1	-	USB D- signal
USB_VBUS0	B Analog	-	1	-	OTG function not supported. Leave this pin floating.
USB_ID0	B Analog	-	1	-	Used to differentiate b/w a mini-A and mini-B plug. USB_ID0 also could be used for analog test signal through internal configuration
USB_TXR_TUNE	B Analog	-	1	-	Transmitter resistor tune pin Connect to 200 ohm (+/-1%) resistor
USB_OVC_B	I LVCMOS	Static	1	PU	USB interface over current indication. Active low.
BOOT_USB_VREG_BYP	I LVCMOS	-	1	PD	0: MSH internal logic uses clock generated from MSH_CLK 1: MSH internal logic uses internal clock. It is recommended to implement compatible design, and the default is pull-down.
CPU_SGMII					
HS_CMU_REFCLK_P/N	I LVDS	156.25MHz	2	-	Reference clock input, typical 156.25MHz
HS_TX_P[1:0] HS_TX_N[1:0]	O CML, 1.0V	3.125Gbps	4	-	Differential Tx Data 1.25Gbps ~ 3.125Gbps
HS_RX_P[1:0] HS_RX_N[1:0]	I CML, 1.0V	3.125Gbps	4	-	Differential Rx Data 1.25Gbps ~ 3.125Gbps
HS_CMU_REXT10K	O LVCMOS	static	1	-	Reserve Pin Should connect to via or keep

Pin Name	Type	Rate	Pin #	PU/ PD	Description
					floating.
SOC I²C Interface					
SCL_SOC[1:0]	B OD	0~400KHz	2	-	SCL_SOC[1] is only for internal CPU. SCL_SOC[0] is duplexed pin which can be used for Internal CPU or switch core for data transfer by I²C interface.
SDA_SOC[1:0]	B OD	0~400KHz	2	-	SDA_SOC[1] is only for internal CPU. SDA_SOC[0] is duplexed pin which can be used for Internal CPU or switch core for data transfer by I²C interface.
SOC SMI Interface					
MDC_SOC	O LVCMOS	0~25MHz	1	-	CPU Subsystem 1G PHY MDIO clock
MDIO_SOC	B LVCMOS	0~25MHz	1	-	CPU Subsystem 1G PHY MDIO data
Watchdog Interface					
WDT0_RST_B	O LVCMOS	-	1	-	Reset Watchdog. Active low.
WDT1_RST_B	O LVCMOS	-	1	-	Reset Watchdog. Active low.
CORE reference clock					
CORE_REFCLK_P CORE_REFCLK_N	I LVDS	50MHz	2	-	Differential input reference clock for Core PLL, typical 50MHz
I²C Master Interface					
MSCL[0:1]	O OD	400KHz	2		I²C Master SCL out, up to 400KHz, default is 100KHz
MSDA[0:1]	B OD	400KHz	2		I²C Master SDA, related with MSCL0~1.
SMI Interface					
MDC_A[1:0]	O LVCMOS 1.2V/3.3V	0-25MHz	2	-	External PHY MDIO clock, compatible with 1G/10G PHY
MDIO_A[1:0]	BLVCMOS 1.2V/3.3V	0-25MHz	2	-	External PHY MDIO data, compatible with 1G/10G PHY
MDC_B[1:0]	O LVCMOS 1.2V/3.3V	0-25MHz	2	-	External PHY MDIO clock, compatible with 1G/10G PHY
MDIO_B[1:0]	BLVCMOS 1.2V/3.3V	0-25MHz	2	-	External PHY MDIO data, compatible with 1G/10G PHY
Synchronous Ethernet Interface					

Pin Name	Type	Rate	Pin #	PU/ PD	Description
RECV_CLK[0:2]	O LVCMOS 1.8V/3.3V	0-150MHz	3	-	Synchronous Ethernet recovery clock, the typical frequencies refer to chapter 10.2. 1.25G~10.3125Gbps: 1.953125MHz 25.78125Gbps: 0.9765625MHz
LED Interface					
LED_CLK	O LVCMOS	25MHz	1	-	Led clock out.
LED_DATA	O LVCMOS	25MHz	1	-	Led data out.
Thermal Interface					
THM_VINS0	I analog	-	1		Used for THM INL/DNL testing, floating in function mode.
THM_VREFP	I analog	-	1		Used for trimming, floating in function mode.
MISC Interface					
FUSE_DONE	O LVCMOS	-	1	-	If assert, indicate the fuse download procedure is finished.
FUSE_FAIL	O LVCMOS	-	1	-	If assert, it indicates that the fuse download procedure is failed.
DEBUG[7:0]	O LVCMOS 1.8V	0- 150MHz	8		Used for chip function debugging; Connect to debug tap on board.
DEBUG_MODE[2:0]	I LVCMOS 1.8V	-	3	PD	Debug mode selection; Connect to debug tap onboard; The internal pull-down resistor ranges from 61K kΩ to 196 kΩ (typical value is 104K kΩ)
IEEE1588 Time Stamp Interface					
PTP_REFCLK_P PTP_REFCLK_N	I LVDS	125M/250MHz	2	-	IEEE1588 Time stamp Engine Differential clock input, maximum frequency is 250MHz.
TOD_REFCLK	I LVCMOS 1.8V	96MHz	1	-	Time of Date interface reference clock input, typical 96MHz
TOD_CODE	B LVCMOS	0-25MHz	1	PU	Obey the CMCC High Precision Time Sync Spec Ver1.0, typical baud rate is 9600bps, indicate the Time of Date.
TOD_PULSE	B LVCMOS	0-25MHz	1	PD	Typical 1pps assertion.
SYNC_CLK	B LVCMOS	0-25MHz	1	PD	TsEngine sync clock, up to 25MHz.

Pin Name	Type	Rate	Pin #	PU/ PD	Description
SYNC_PULSE	B LVCMOS	0-25MHz	1	PD	TsEngine sync pulse.
SYNC_CODE	B LVCMOS	0-25MHz	1	PD	TsEngine sync code.
Interrupt Interface					
INTR_B[3:0]	O LVCMOS	-	4	-	Interrupt output signals. Active low.
JTAG Interface					
TCK	I LVCMOS	25MHz	1	PU	JTAG Clock input.
TRST_B	I LVCMOS	25MHz	1	PD	JTAG Test Reset. This signal is active low.
TMS	I LVCMOS	25MHz	1	PU	JTAG Test Mode Select input.
TDI	I LVCMOS	25MHz	1	PU	JTAG Data input.
TDO	O LVCMOS	25MHz	1	-	JTAG Data output.

Table 8-2 : Pin information –Power and Ground

Pin Name	Type	Rate	Pin #	Description
Power				
VDD	I 0.9V	Core Power		VDD core power supply (0.9V typ)
VDDIO3312_MDIO_A	I 3.3V or 1.2V	MDIO_A IO Power		MDIO_A IO power supply (3.3V or 1.2V typ)
VDDOUT_MDIO_A	O	Power Filter		MDIO_A Power Filter, connect to 1.0uF capacitor
VDDIO3312_MDIO_B	I 3.3V or 1.2V	MDIO_B IO Power		MDIO_B IO power supply (3.3V or 1.2V typ)
VDDOUT_MDIO_B	O	Power Filter		MDIO_B Power Filter, connect to 1.0uF capacitor
VDDIO33	I 3.3V	3.3V IO power		3.3V IO power supply (3.3V typ)
VDDOUT_G{1..5}	O	Power Filter		3.3V IO power filter, connect to 1.0uF capacitor
VDDIO3318_GPIO_7_0	I 3.3V or 1.8V	GPIO{0..7} Power		GPIO{0..7} 3.3V power supply (3.3V typ)
VDDOUT_GPIO_7_0	O	Power Filter		GPIO{0..7} power filter, connect to 1.0uF capacitor
VDDIO3318_RECV	I 3.3V or 1.8V	RECV Power		Recovery clocks IO 3.3V power supply (3.3V typ)
VDDOUT_RECV	O	Power Filter		Recovery clocks IO power filter, connect to 1.0uF capacitor
VDDIO3318_MSH	I 3.3V or 1.8V	MSH Power		eMMC IO 3.3V power supply (3.3V typ)

Pin Name	Type	Rate	Pin #	Description
VDDOUT_MSH	O	Power Filter		eMMC IO power filter, connect to 1.0uF capacitor
AVDD18_THM	I 1.8V	Analog Power	1	Thermal analog power supply (1.8V typ)
AVDD18_DDRPLL	I 1.8V	Analog Power	1	Analog power 1.8V for the PLL for DDR PHY (1.8v typ), corresponding GND is AVSS_DDRPLL
VDD09_DDRPLL	I 0.9v	Analog Power	1	Digital power 0.9V for the PLL for DDR PHY (0.9v typ), corresponding GND is VSS_DDRPLL
AVDD18_PLL	I 1.8v	Analog Power	1	Analog power 1.8V for the PLLs of Core/Sup/SoC (1.8v typ), corresponding GND is AVSS_PLL
VDDIO18	I 1.8v	1.8V IO Power		Digital Power supply for 1.8V IO (1.8v typ)
AVDD18_PCIE	I 1.8v	Analog Power		Analog Power 1.8V for PCIe PHY, corresponding GND is AVSS_PCIE
AVDD09_PCIE	I 0.9v	Analog Power		Analog Power 0.9V for PCIe PHY, corresponding GND is AVSS_PCIE
AVDD09_VCO_PCIE	I 0.9v	Analog Power		Analog Power 0.9V for PCIe PHY VCO, corresponding GND is AVSS_PCIE
AVDD09_HS0 AVDD09_HS1 AVDD09_HS2	I 0.9v	Analog Power		Analog Power 0.9V for 8x Lanes HSS12G SerDes hard macro (0.9v typ)
AVDD09_VCO_HS0 AVDD09_VCO_HS1 AVDD09_VCO_HS2	I 0.9v	Analog Power		Analog Power 0.9V for 8x Lanes HSS12G SerDes VCO (0.9v typ)
AVDD18_HS0 AVDD18_HS1 AVDD18_HS2	I 1.8v	Analog Power		Analog Power 1.8V for 8x Lanes HSS12G SerDes hard macro (1.8v typ)
AVDD09_HS3	I 0.9v	Analog Power		Analog Power 0.9V for SoC 2x Lanes HSS12G SerDes hard macro (0.9v typ)
AVDD09_VCO_HS3	I 0.9v	Analog Power		Analog Power 0.9V for SoC 2x Lanes HSS12G SerDes VCO (0.9v typ)
AVDD18_HS3	I 1.8v	Analog Power		Analog Power 1.8V for SoC 2x Lanes HSS12G SerDes hard macro (1.8v typ)
AVDD18_CS	I 1.8v	Analog Power		Analog Power 1.8V for 4x Lanes HSS28G SerDes hard macro (1.8v typ)
AVDD18_ADD_DDR	I 1.8v	Analog Power		Analog Power 1.8V for DDR PHY address (1.8v typ), corresponding GND is AVSS18_ADD_DDR
AVDD18_DATA_H8_DDR	I 1.8v	Analog Power		Analog Power 1.8V for DDR PHY MSB 8bit Data (1.8V typ), corresponding GND is AVSS18_DATA_H8_DDR

Pin Name	Type	Rate	Pin #	Description
AVDD18_DATA_L16_DDR	I 1.8v	Analog Power		Analog Power 1.8V for DDR PHY LSB 16bit Data (1.8V typ), corresponding GND is AVSS18_DATA_L16_DDR
VDDIO_DDR	I 1.2v or 1.35v or 1.5v	Power		Digital power supply for DDR IO - 1.2VDDR4 - 1.35VDDR3L - 1.5VDDR3
VDDIO_DDR_CK	I 1.2v or 1.35v or 1.5v	Power		Digital power supply for DDR Clock IO - 1.2VDDR4 - 1.35VDDR3L - 1.5VDDR3
VDD_USB	I 0.9v	Power		Digital Power supply for USB PHY
AVDD33_USB	I 3.3v	Analog Power		Analog Power supply for USB PHY (3.3v typ)
AVDD18_LVDS	I 1.8v	Analog Power		Analog Power supply for LVDS IO (1.8v typ)
VDDIO18_EFUSE_INFO	I 1.8v	Power		Digital power supply for 32x32b customized eFUSE. MUST connect to GND through resistor(1kΩ) in function mode.
VDDIO18_EFUSE_MEM	I 1.8v	Power		Digital power supply for 128x32b memory eFUSE. MUST connect to GND through resistor(1kΩ) in function mode.
GROUND				
VSS	I	GND		Digital ground
AVSS_DDRPLL	I	GND		Analog ground for AVDD18_DDRPLL
VSS_DDRPLL	I	GND		Ground for VDD09_DDRPLL
AVSS_PLL	I	GND	3	Analog ground for AVDD18_PLL
AVSS_PCIE	I	GND		Analog ground for PCIe PHY
AVSS18_ADD_DDR	I	GND		Analog ground for AVDD18_ADD_DDR
AVSS18_DATA_H8_DDR	I	GND		Analog ground for AVDD18_DATA_H8_DDR
AVSS18_ADD_L16_DDR	I	GND		Analog ground for AVDD18_DATA_L16_DDR

9 Electrical Specifications

9.1 Absolute Maximum Rating

CAUTION

Stress above the specification listed in Table 9-1 may cause permanent damage to the device. Function operation is not guaranteed under or above these conditions. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 9-1 : Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD[1]	Core digital 0.9V power Supply	-0.18	1.08	V
VDD09_DDRPLL	Digital 0.9V power supply for the PLL for DDR PHY	-0.18	1.08	V
AVDD09*	Analog 0.9V Power Supply	-0.18	1.08	V
AVDD18*	Analog 1.8V Power Supply	-0.36	1.98	V
VDDIO18*	Digital 1.8V Power Supply	-0.36	1.98	V
VDDIO33*	Digital Power Supply for 3.3V IO	-0.5	3.80	V
VDDIO3312*	Digital Power Supply for 3.3V/1.2V compatible IO	-0.5	3.80 1.38	V
VDDIO3318*	Digital Power Supply for 3.3V/1.8V compatible IO	-0.5	3.80 1.98	V
VDDIO_DDR*	Digital IO Power Supply for DDR IO - 1.2V (DDR4) - 1.35V (DDR3L) - 1.5V (DDR3)	-0.5	1.38 1.5525 1.725	V
$V_{DV/DT}$[2]	Supply Voltage Slew Rate	-	18	V/ms
T_{ST}	Storage Temperature	-40	125	°C
Tj	Junction Temperature	-	125	°C
Ta	Ambient operating temperature range	-40	85	°C
HBM	JS-001-2014 JEP-155	-	1000	V
CDM	JS-002-2014 JEP-157	-	250	V

NOTE

Note[1]: Limited by 12G LVDS RX Digital VDD absolute maximum ratings.

Note[2]: Limited by 1.8V GPIO

9.2 Recommended Operating Conditions

Recommended operating conditions are values that guarantee correct device operation.Aslong as the device is used within the ranges, electrical characteristics (DC and AC characteristics) are guaranteed.

Table 9-2 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Tolerance(use forTyp) (AC+DC)	Unit
VDD[1]	Core digital 0.9V power Supply	0.873	0.900	0.927	±3%	V
VDD09_DDRPLL	Digital 0.9V power supply for the PLL for DDR PHY	0.873	0.900	0.927	±3%	V
AVDD09*	Analog 0.9V Power Supply	0.873	0.900	0.927	±3%	V
AVDD18*	Analog 1.8V Power Supply	1.710	1.800	1.890	±5%	V
VDDIO18*	Digital 1.8V Power Supply	1.710	1.800	1.890	±5%	V
VDDIO33*	Digital Power Supply for 3.3V IO	3.135	3.300	3.465	±5%	V
VDDIO3312*	Digital Power Supply for 3.3V/1.2V compatibleIO	3.135 1.140	3.300 1.200	3.465 1.260	±5%	V
VDDIO3318*	Digital Power Supply for 3.3V/1.8V compatibleIO	3.135 1.62	3.300 1.80	3.465 1.98	±5%	V
VDDIO_DDR*	Digital IO Power Supply for DDR IO - 1.2V (DDR4) - 1.35V (DDR3L) - 1.5V (DDR3)	1.140 1.283 1.425	1.200 1.350 1.500	1.260 1.417 1.575	±5%	V
Tj[2]	Junction Temperature	0		110		°C
Ta	Ambient operating temperature range	-10		70		°C

NOTE

Note*: All voltages are probed from package BGA BALL.

Note[1]: VDD tolerance ±3%, AC ripple MUST be less than 20mVpp from DC to 100MHz (Limited by PCIe PHY).

Note[2]: Operation condition of Tj is limited by PCIe PHY and HSS28G SerDes

Consider the minimum number of voltage supply number and the minimum power consumption of 5VT6126, the recommended power supply as the following table: Table 9-3

Table 9-3 : Recommended Power Supply

Power Type/Power Module	Voltage (Typical)	Tolerance (Minimum) (AC+DC)	Unit
VDD	0.900	±3%	V
VDD09_DDRPLL AVDD09*	0.900	±3%	V
AVDD18* VDDIO18* VDDIO3318* (1.8V mode)	1.800	±5%	V
VDDIO33* VDDIO3318* (3.3V mode) VDDIO3312* (3.3V mode)	3.300	±5%	V
VDDIO3312* (1.2V mode) VDDIO_DDR* (DDR4 mode) [1]	1.200	±5%	V

NOTE

Note[1]: DDR IO could use 1.5V for DDR3 or 1.35V for DDR3L.

9.3 Power-Up and Power-Down Specifications

Table 9-4 : Power Up and Power Off Timing Parameters

Symbol	Description	Min	Max	Units
tDELAY1	0.9V power up to 1.2V/1.35V/1.5V power up delay 1.2V/1.35V/1.5V power off to 0.9V power off	200	-	us
tDELAY2	1.2V/1.35V/1.5V power up to 1.8V power up delay 1.8V power off to 1.2V/1.35V/1.5V power off	200	-	us
tDELAY3	1.8V power up to 3.3V power up delay 3.3V power off to 1.8V power off	20	-	us
tSLEW	Power Ramp Up Slew	200	10000	us
Zpwr	Power supply Impedance (DC ~ 100MHz)	-	40	mOhm

0.9V

1.2/1.35/1.5V

1.8V

3.3V

NOTE

The detailed information about Boot Up/Reset Sequence, please refer to 5VT6126_Advanced_Hardware_Design_Guide.

9.4 Boot Up/Reset Sequence

NOTE

The detailed information about Boot Up/Reset Sequence, please refer to 5VT6126_Advanced_Hardware_Design_Guide.

9.5 Power Supply and Power Consumption

The following power consumptions based on different bandwidth (i.e different core frequency and configuration mode) are estimated.

Table 9-5 :Maximum Power Consumption Estimation

Mode	I/O Bandwidth	Junction Temp (°C)	VDD (V)	*AVDD18 (V)	*AVDD09 (V)	Max (Watts)
24x10G + 8x25G/2x100G	440Gbps	110	0.927	1.890	0.927	41.13
24x10G + 2x40G	320Gbps	110	0.927	1.890	0.927	36.32
48 x 1G + 8 x 10G	128Gbps	110	0.927	1.890	0.927	28.06
24 x 1G + 2 x 40G	104Gbps	110	0.927	1.890	0.927	26.23
32 x 1G +4 x 10G	72Gbps	110	0.927	1.890	0.927	24.14

NOTE

The maximum power consumption estimation does not include the CPU's.

Table 9-6 : Typical Power Consumption Estimation

Mode	I/O Bandwidth	Junction Temp (°C)	VDD (V)	*AVDD18 (V)	*AVDD09 (V)	Typical (Watts)
24x10G + 8x25G/2x100G	440Gbps	65	0.900	1.800	0.900	22.65
24x10G + 2x40G	320Gbps	65	0.900	1.800	0.900	22.36
48 x 1G + 8 x 10G	128Gbps	65	0.900	1.800	0.900	19.64
24 x 1G + 2 x 40G	104Gbps	65	0.900	1.800	0.900	18.36
32 x 1G +4 x 10G	72Gbps	65	0.900	1.800	0.900	16.9

NOTE

The typical power consumption estimation does not include the CPU's.

For PSU and thermal designing, the following power requirement for different voltage rails are provided based on 24x10GE+2x100GE, total 440Gbps, other configuration mode could use different number proportionally.

The power requirements of different voltage rails for 440Gbps are listed in the following table.

Table 9-7 : Power Requirement for Different Voltage Jc=110 °C (Estimation)

Power Type	Voltage	Tolerance (Min) (AC+DC)	Watts (Max)	Current (Max) Unit: A	Percentage (Subtotal/ Total Pwr)
VDD	0.900	±3%	29.300	32.56	65.64%
AVDD09*	0.900	±3%	5.205	5.783	11.66%
AVDD18*	1.800	±5%	5.818	3.232	13.03%
AVDD33_USB/ VDDIO33*	3.300	±5%	1.500	0.455	3.36%
VDDIO_DDR*[1]	1.500 or 1.2 or 1.35 or	±5%	1.825 or 1.168 or 1.479	1.217or 0.973or 1.095	4.14%
VDDIO3312*	1.200	±5%	0.43	0.358	0.98%

NOTE

Note1: VDDIO_DDR* use 1.20V (DDR4) or 1.35V (DDR3L) or 1.50V (DDR3)

9.6 Interface I/O DC Specifications

9.6.1 3.3V General I/O Specifications

These specifications apply to 3.3V LVCMOS I/O signals.

Table 9-8 : 3.3V LVCMOS driver/receiver dc specification:

Symbol	Parameter	Min	Typ.	Max	Units
V_{IL}	DC Input Logic Low	-0.300	-	0.825	V
V_{IH}	DC Input Logic High	2.063	-	3.6	V
V_{OL}	DC Output Logic Low	-	-	0.413	V
V_{OH}	DC Output Logic High	2.475	-	-	V
I_{OZ}	Tristate Output Leakage Current			±10	uA
I_I	Input Leakage Current			±10	uA
I_{OL}	Low Level Output Current @V_{OL} (max)	6.8	13.2	23.9	mA
I_{OH}	High Level Output Current @V_{OH} (min)	10.9	18.9	33.5	mA

Symbol	Parameter	Min	Typ.	Max	Units
Freq.	IO frequency			50.0	MHz

9.6.2 1.8V General I/O Specifications

These specifications apply to 1.8V LVCMOS I/Osignals.

Table 9-9 : 1.8V LVCMOS driver/receiver dcspecification

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	DC Input Logic Low	-0.30	-	0.63	V
V_{IH}	DC Input Logic High	1.17	-	1.98	V
V_{OL}	DC Output Logic Low	-	-	0.45	V
V_{OH}	DC Output Logic High	1.35	-	-	V
I_{OZ}	Tristate Output Leakage Current			±10	uA
I_I	Input Leakage Current			±10	uA
I_{OL}	Low Level Output Current @V_{OL} (max)	11.1	18.2	25.6	mA
I_{OH}	High Level Output Current @V_{OH} (min)	13.1	19.1	26.3	mA
Freq.	IO frequency			150.0	MHz
CI	Capacitance Pad to GND		1.18		pF

9.6.3 3.3V I²C I/O Specifications

These specifications apply to 3.3V I²C I/O signals.

Table 9-10 : 3.3V I²C I/O dc specification

Symbol	Parameter	Min	Typ.	Max	Units	Comments
V_{IL}	DC Input Logic Low	-0.500	0	0.800	V	
V_{IH}	DC Input Logic High	2.195	3.300	3.6	V	
V_{OL}	DC Output Logic Low	0	-	0.4	V	@I_{OL} =3mA
I_{OZ}	Tristate Output Leakage Current @Vo=3.3V or 0V	-10		10	uA	@V_O= 3.3V or 0V
I_I	Input Leakage Current 0V < V_I< 3.465V	-10		10	uA	0V < V_I< 3.465V
Freq.	IO frequency			400K	Hz	
CI	Capacitance of each I/O pin (Pad to GND)			10	pF	

9.6.4 1.2V/3.3V MDIO I/O Specifications

These specifications apply to 1.2V/3.3V MDIO I/O signals

Table 9-11 : 1.2V/3.3V MDIO DC specification (**VDD_{IO} = 1.2V**)

Symbol	Parameter	Min	Typ.	Max	Units	Comments
V_{IL}	DC Input Logic Low	-	-	0.52	V	
V_{IH}	DC Input Logic High	0.77	-	-	V	
V_{OL}	DC Output Logic Low	-	-	0.20	V	
V_{OH}	DC Output Logic High	1.00	-	-	V	
I_{OL}	Low Level Output Current @V_{OL} (max)	4.0	-	6.7	mA	
I_{OH}	High Level Output Current @V_{OH} (min)	4.0	-	7.2	mA	
Freq.	Operating Frequency			25	MHz	

NOTE

Note: 1.2V/3.3V MDIO DC spec is the same as 3.3V only IO while VDD_{IO}=3.3V

9.6.5 1.8V/3.3V eMMC I/O Specifications

These specifications apply to 1.8V/3.3V eMMC I/O signals

Table 9-12 : 1.8V/3.3V eMMC specification (**VDD_{IO} = 1.8V**)

Symbol	Parameter	Min	Typ.	Max	Units	Comments
V_{IL}	DC Input Logic Low	-0.30	-	0.58	V	
V_{IH}	DC Input Logic High	1.27	-	1.98	V	
V_{OL}	DC Output Logic Low	-	-	0.45	V	
V_{OH}	DC Output Logic High	1.40	-	-	V	
I_{OL}	Low Level Output Current @V_{OL} (max)	6.7	11.4	16.7	mA	
I_{OH}	High Level Output Current @V_{OH} (min)	3.8	9.4	17.7	mA	
Freq.	Operating Frequency (VDD_{IO} = 1.8V)			150	MHz	

NOTE

Note: 1.8V/3.3V MDIO DC spec is the same as 3.3V only IO while VDD_{IO}=3.3V

9.6.6 LVDS I/O Specifications

Table 9-13 : LVDS I/O receiver dc specification

Symbol	Parameter	Min	Typ.	Max	Units

Symbol	Parameter	Min	Typ.	Max	Units
NVDD1	Analog Supply Voltage	1.62	1.80	1.98	V
I_{dda}	Analog Supply Current	-	5	-	mA
I_{ddd}	Digital Supply Current	-	1	-	mA
R_{term}	RX internal termination resistance	50	100		Ohm
V_I	RX input range	0		NVDD1	V
V_t	RX input differential threshold	-200	-	+200	mV
Freq	Data rate	-	-	500	Mbps

9.6.7 DDR3/4 I/O Specifications

Table 9-14 : DDR3/4 I/O dc specification

Symbol	Parameter	Min	Typ.	Max	Units
VDDIO_DDR VDDIO_DDR_CK	DDR3 IO post-driver power	1.425	1.5	1.575	V
	DDR4 IO post-driver power	1.14	1.2	1.26	V
AVDD18_*_DDR	1.8V analog Power	1.71	1.80	1.89	V

9.6.8 HSS 28G SerDes Electrical Specifications

Unless otherwise specified, the Table 9-15 characteristics are met while operating within the Normal Range of Operating conditions. These specifications apply at 5VT6126 BGA balls.

Table 9-15 : HSS28G SerDes Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
Vdiff-out	Output Differential Voltage Range	Programmable	200	-	1000	mVp-p
TEQS	Output Equalization Coefficient Step Size	Normalized, Equalization on	1.5	-	5	%
TRF	Output Rise/Fall Time	20~80%	8			Ps
TTJ	Output Total Jitter				0.21	UI
VCM	Output Common Mode Voltage			0.45		V
R_TX	TX output impedance		80	100	120	Ohm
VCMN	Input Common Mode Noise				12	mV-rms
Vdiff-in	Input differential Voltage		50		1200	mVp-p
R_RX	RX Input Resistance		80	100	120	Ohm
LAT_RX	Full-rate mode RX latency			2.8		ns
LAT_TX	Full-rate mode TX latency			3.6		ns

9.6.9 HSS12G SerDes Electrical Specifications

Unless otherwise specified, the following characteristics are met while operating within the Normal Range of Operating condition. These specifications apply at the module BGA ball.

Table 9-16 : HSS12G SerDes Absolute Maximum Ratings

Parameter	Description	Max	Unit
V_{INPUT}	Digital Input signal Voltage Level	1.1	V
V_{OUTPUT}	Digital Output signal Voltage Level	1.1	V

10 ACTiming

10.1 Clock Source Supply

The table lists the requirement of the reference clock.

Table 10-1 Characteristics of the SerDes interfaces reference clock

Seq#	PIN Name	TYPE	Description	Requirement
1	HS_S0/1/2_REFCLK_P/N	I LVDS	12.5G Serdes macro#0/1/2 reference clock	• Freq：156.25MHz±50ppm • Dutycycle：40~60% • jitter: 1.0psrms[2] • Rise/Fallrate(20%~80%): • 1V/ns~4V/ns • Input voltage:400~1600mV
2	CS_REFCLK_P/N	I LVDS	28G Serdes macro#0/1 reference clock	• Freq：156.25MHz±50ppm • Dutycycle：45~55% • jitter: 1.0psrms[2] • Rise/Fall time(20~80%): 0.1ns~0.5ns • Input voltage:350~1200mV
3	HSS_REFCLK_P/N[1]	I LVDS	External Reference clock to generate sup clock for 28G Serdes and super control logic. HSS_REFCLK is necessary for chip boot up.	• Freq：156.25MHz±50ppm • Dutycycle：45~55% • jitter: 1.0psrms[2] • Rise/Fall time (20~80%):0.1ns~0.75ns • Input voltage:350~1200mV
4	HS_CMU_REFCLK_P/N	I LVDS	CPUMAC SGMII reference clock	• Freq：156.25MHz±50ppm • Dutycycle：40~60% • jitter: 1.0psrms[2] • Rise/Fallrate(20~80%): • 1V/ns~4V/ns • Input voltage:400~1600mV
5	CORE_CLK_P/N	I LVDS	CORE reference clcok	• Freq：50MHz±50ppm • Dutycycle：40~60% • jitter: 2.0psrms[3] • Rise/Fall time (20~80%):0.25ns~0.75ns • Input voltage:400~1600mV

Seq#	PIN Name	TYPE	Description	Requirement
6	PCIe_REFCLK_P/N	I HCSL	PCIe reference clcok	• Freq：100MHz±100ppm • Refer to PCIe2.0Standard • Jitter: SeeNote[4]
7	PTP_CLK_P/N	I LVDS	PTP reference clock	• Freq：125/250MHz±4.6ppm • Dutycycle：40~60% • Jitter: ±100ps(c2c)[5] • Rise/Fall time (20~80%):0.1ns~0.75ns • Input voltage:400~1600mV
8	TOD_REFCLK	I 1.8V CMOS	TOD reference clock	• Freq：96MHz±100ppm • Dutycycle：40~60% • Jitter:±200ps(c2c) • Rise/Fall time (20~80%):0.1ns~0.75ns
9	FCIN_CLK	I 1.8V CMOS	External FlowControl reference clock	• Freq：125MHz±100ppm • Dutycycle：40~60% • Jitter:±200ps(c2c) • Rise/Fall time (20~80%):0.25ns~0.75ns

NOTE

Note[1]: HSS_REFCLK_P/N and CS_REFCLK_P/N MUST use exam same clock source, i.e clock generator or oscillator.

Note[2]: Random Jitter 50KHz ~10MHz

Note[3]: PLL external input reference clock jitter is long term RMS jitter from 10kHz to Fref/10 < 2ps, the value of Fref=50MHz.

Note[4]: PCIe 100MHz reference clock requirements refer to the PCIe SIG spec.

Note[5]: Frequency tolerance is ±4.6ppm.

Table 10-2 : HSS12G SerDes External Reference Clock Requirements

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
$T_{C\text{-}RISE}$	Rising edge rate	Differential	1.0	-	4.0	V/ns
$T_{C\text{-}FALL}$	Falling edge rate	Differential	1.0	-	4.0	V/ns
V_{DIFF}	Differential Input Swing	Differential	400	-	1600	mV
V_{RB}	Ring Back Voltage Margin	Differential	-50	-	+50	mV
T_{STABLE}	Time Before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD\text{-}AVG}$	Average Clock Period Accuracy	Differential	-100	-	+100	ppm
F_{REF}	Reference Clock Freq.			156.25 or 61.13		MHz
DUTY	Duty Cycle	Differential	40		60	ohm
RJ	Random Jitter 50KHz ~10MHz				1.0	ps rms

Table 10-3 : HSS28G SerDes External Reference Clock Requirements

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
NTPS	Supply Noise Tolerance	50Hz to 5.0GHz		20		mVp-p
CLKIV	Clock Differential Input Voltage		350	-	1200	mVp-p
CLKIDC	Clock Input Duty Cycle		45	-	55	%
CLKIRF	Clock Input Rise/Fall Time				500	Ps
CLKIJITTER	Clock RMS Noise				1	ps

Table 10-4 : PCIe Reference Clock Jitter and Swing Requirement

Application	Reference Clock Jitter and Swing Requirement
PCIe 2.5 Gbps	For requirements, refer to the PCI Express 1.0 Card Electrometrical specification
PCIe 5.0 Gbps	For requirements, refer to the PCI Express 2.0 base specification

10.2 Recovery Clock Output

Table 10-5 : SerDes Recovery Clock Output Frequency

SerDes Type	Data Rate (Gbps)	Baud Rate (Gbps)	Enc/Dec	Recovery clock Frequency (MHz)	Divider	Output Clock Frequency (MHz)
12.5G SerDes	1	1.25	8b/10b	125	64	1.953125
12.5G SerDes	2.5	3.125	8b/10b	312.5	160	1.953125
12.5G SerDes	10	10.3125	64b/66b	322.265625	165	1.953125
28G SerDes	1	1.25	8b/10b	39.0625	20	1.953125
28G SerDes	2.5	3.125	8b/10b	97.65625	50	1.953125
28G SerDes	10	10.3125	64b/66b	322.265625	165	1.953125
28G SerDes	25	25.78125	64b/66b	805.6640625	825	0.9765625

10.3 I²C Interface Timing Parameter

Table 10-6 : Characteristics of the SDA and SCL for S-mode, from THE I 2C-BUS SPECIFICATION

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		Units
		MIN	MAX.	MIN	MAX.	
		-		-		
SCL Clock frequency	f_{SCL}	0	100	0	400	kHz

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		Units
		MIN	MAX.	MIN	MAX.	
Hold time(repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	4.0	–	0.6	–	µs
LOW period of SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU,STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters for I²C-bus devices	$t_{HD,DAT}$	5.0 0	– 3.45	– 0	– 0.9	µs
Data set-up time	$t_{SU,DAT}$	250	–	100	–	µs
Rise time of both SDA and SCL signals	t_r	–	1000	$20+0.1C_b$	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20+0.2C_b$	300	ns
Set-up time for STOP condition	$t_{SU,STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1VDD	–	0.1VDD	–	V
Noise margin at the High level foreach connected device (includinghysteresis)	V_{nH}	0.2VDD	–	0.2VDD	–	V

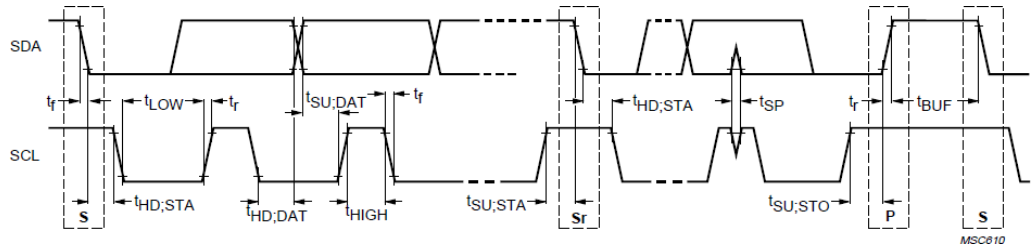

Figure 10-1 : Definition of timing of I²C

10.4 MDC/MDIO Interface Timing

Table 10-7 : MDC/MDIO Interface Timing Parameters

Symbol	Signals	Description	Min	Max	Units
F_{MDC}	MDC_*	MDC clock frequency	-	25	MHz

Symbol	Signals	Description	Min	Max	Units
DC_{MDC}	MDC_*	MDC clock duty cycle	40	60	%
T_{SU}	MDIO_*	MDIO input Setup time	10	-	nS
T_{HD}	MDIO_*	MDIO input Hold time	0	-	nS
T_{OSU}	MDIO_*	MDIO output Setup time	10	-	nS
T_{OH}	MDIO_*	MDIO output Hold time	10	-	nS

Figure 10-2 : MDC/MDIO Input Timing Diagram

Figure 10-3 : MDC/MDIO Output Timing Diagram

10.5 OOBFC Interface Timing Parameter

Table 10-8 : OOBFC Interface Timing Parameters

Symbol	Signals	Description	Relative to Clock	Min	Max	Units
F	FCIN_CLK FCOUT_CLK	Flow control clocks	N/A	-	125	MHz
DC	FCIN_CLK FCOUT_CLK	Flow clock duty cycle	N/A	40	60	%
T_{SU}	FCIN_DATA FCIN_SYNC	Setup time	FCIN_CLK	1	-	nS
T_{HD}	FCIN_DATA	Hold time	FCIN_CLK	1	-	nS

Symbol	Signals	Description	Relative to Clock	Min	Max	Units
	FCIN_SYNC					
T_{OSU}	FCOUT_DATA FCOUT_SYNC	Flow control output setup time	FCOUT_CLK	1	-	nS
T_{OH}	FCOUT_DATA FCOUT_SYNC	Flow control output hold time	FCOUT_CLK	1	-	nS

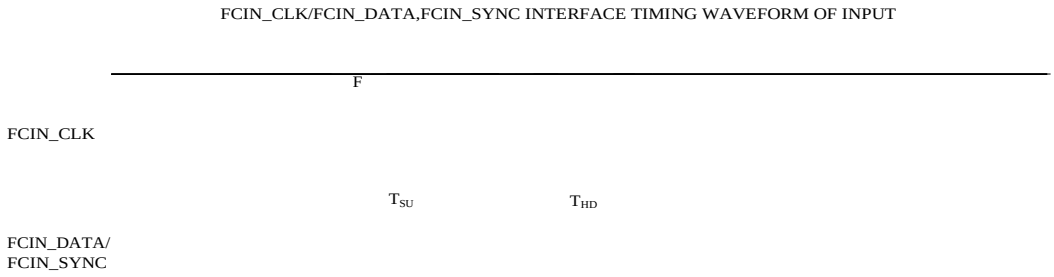

Figure 10-4 : FCIN_* Signals Input Timing Diagram

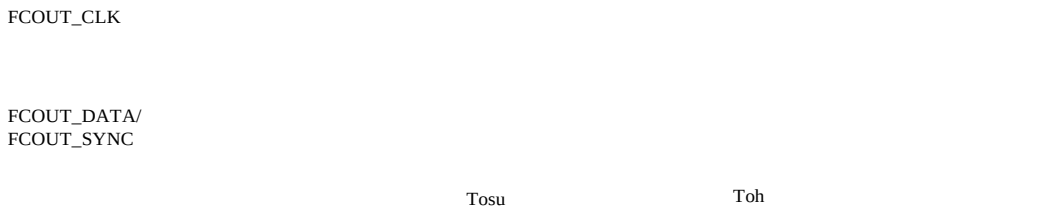

Figure 10-5 : FCOUT_* Signals Output Timing Diagram

10.6 LED Interface Timing Parameter

Table 10-9 : LED Interface Timing Parameters

Symbol	Signals	Description	Relative to Clock	Min	Max	Units
Freq	LEDCLK	LED clocks	N/A	-	25	MHz
DC	LEDCLK	LED clock duty cycle	N/A	40	60	%
T_{OSU}	MACLED	MACLED output setup time	LEDCLK	10	-	nS
T_{OH}	MACLED	MACLED output hold time	LEDCLK	10	-	nS

Figure 10-6 : LEDCLK/MACLED Output Timing Diagram

10.7 HSS28G SerDes Signals Specifications

Unless otherwise specified, the Table 9-15 characteristics are met while operating within the Normal Range of Operating conditions. These specifications apply at 5VT6126 BGA balls.

10.8 HSS12G SerDes Signals Specifications

Unless otherwise specified, the Table 9-16 characteristics are met while operating within the Normal Range of Operating conditions. These specifications apply at 5VT6126 BGA balls.

Table 10-10 : HSS12G SerDes TX SignalsCharacteristics

Parameter	Conditions	Min	Typ.	Max	Unit
Differential Output Peak to Peak Voltage		200	-	1200	mVp-p
20~80% rise/fall time		24	-	150	Ps
Differential return loss	1GHz ~ 6GHz	10			dB
Common mode return loss	0.1GHz ~ 6GHz	8			dB
DC output differential termination		80	-	120	ohm
Total Jitter	10.3125Gbps	-	-	20.15	ps
Random Jitter	10.3125Gbps	-	-	600	fs

Table 10-11 : HSS12G SerDes RX SignalsCharacteristics

Parameter	Conditions	Min	Typ.	Max	Unit
Differential Input Peak to Peak Voltage		110		1000	mVp-p
Input Transition time		0.15	-	0.4	UI
Differential return loss	1GHz~6GHz	12			dB
Common mode return loss	0.1GHz~6GHz	6			dB
DC input differential termination		80		120	Ohm
Freq. offset tolerance		-100	0	100	ppm

10.9 QSPI Interface Timing Parameter

Table 10-12 : QSPI Interface Timing Parameters

Symbol	Signals	Description	Min	Typ	Max	Units
fCK	QSPI_CLK	QSPI clock frequency	1	-	25	MHz
tCK	QSPI_CLK	QSPI clock period	40	1/tCK	1000	ns
tWH	QSPI_CLK	QSPI clock high time	0.4 tCK	-	0.6 tCK	nS
tWL	QSPI_CLK	QSPI clock low time	0.4 tCK	-	0.6 tCK	nS
tDO	QSPI_DATA	QSPI data output valid time	-	-	12	nS
tSU	QSPI_DATA	QSPI data Setup time	5		-	nS
tHD	QSPI_DATA	QSPI data Hold time	5		-	nS
tCSS	QSPI_CS[1:0]	QSPI chip select output lead time	1 tCK		-	nS
tCSH	QSPI_CS[1:0]	QSPI chip select output trail time	1 tCK		-	nS

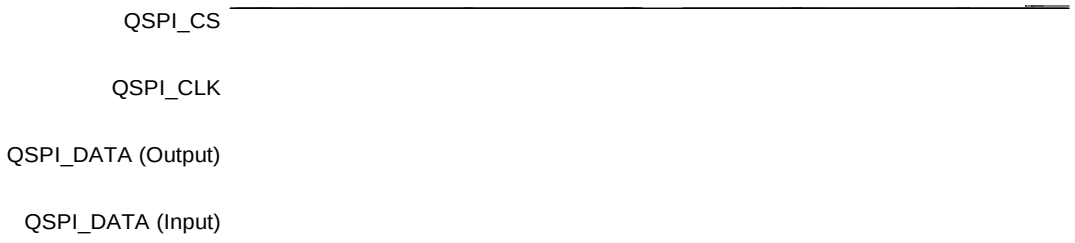

Figure 10-7 : QSPI_* Timing Diagram

10.10 SPI Interface Timing Parameter

Table 10-13 : SPI Interface Timing Parameters

Symbol	Signals	Description	Min	Typ	Max	Units
fCK	SPI_CLK	SPI clock frequency	2	-	25	MHz
tCK	SPI_CLK	SPI clock period	40	1/fCK	500	ns
tWH	SPI_CLK	SPI clock high time	0.4 tCK	-	0.6 tCK	nS
tWL	SPI_CLK	SPI clock low time	0.4 tCK	-	0.6 tCK	nS
tDO	SPI_MOSI	SPI data output valid time relative to SPI_CLK falling edge	-	-	5	nS
tSU	SPI_MISO	SPI data in setup time relative to SPI_CLK rising edge	4.0		-	nS
tHD	SPI_MISO	SPI data in hold time relative to SPI_CLK rising edge	5.0	-	-	nS
tCSS	SPI_CS_B[3:0]	SPI chip select active before	0.5 tCK	-	-	nS

Symbol	Signals	Description	Min	Typ	Max	Units
	SPI_FSS	SPI_CLK active edge				
tCSH	SPI_CS_B[3:0] SPI_FSS	SPI chip select not active after SPI_CLK active edge	0.5 tCK	-	-	nS

Figure 10-8 : SPI Interface Timing Diagram（For mode 3）

10.11 eMMC Interface Timing Parameter

MMC interface support the following speeds, frequencies, and voltages switching.

eMMC

- Backwards Compatibility with legacy MMC card – up to 25MHz,3.3V/1.8V
- High speed SDR – clock up to 50MHz,3.3V/1.8V

Table 10-14 : eMMC Interface Input Timing Parameters

Signal	Input Min Setup Time tISU	Input Min Hold Time tIH
CMD/DATA	0ns	2.0ns

Table 10-15 : eMMC Interface Output Timing Parameters

Speed Mode	Max Freq. fPP	Min Period	Output Min tODLY	Output Max tODLY (ns)
Identification Mode	400KHz	2.5us	-	50.0ns

MMC High Speed SDR (DATA and CMD)	50MHz	20ns	-	8.5ns

Speed Mode	Max Freq. fPP	Min Period	Output Min tODLY	Output Max tODLY (ns)
			-	

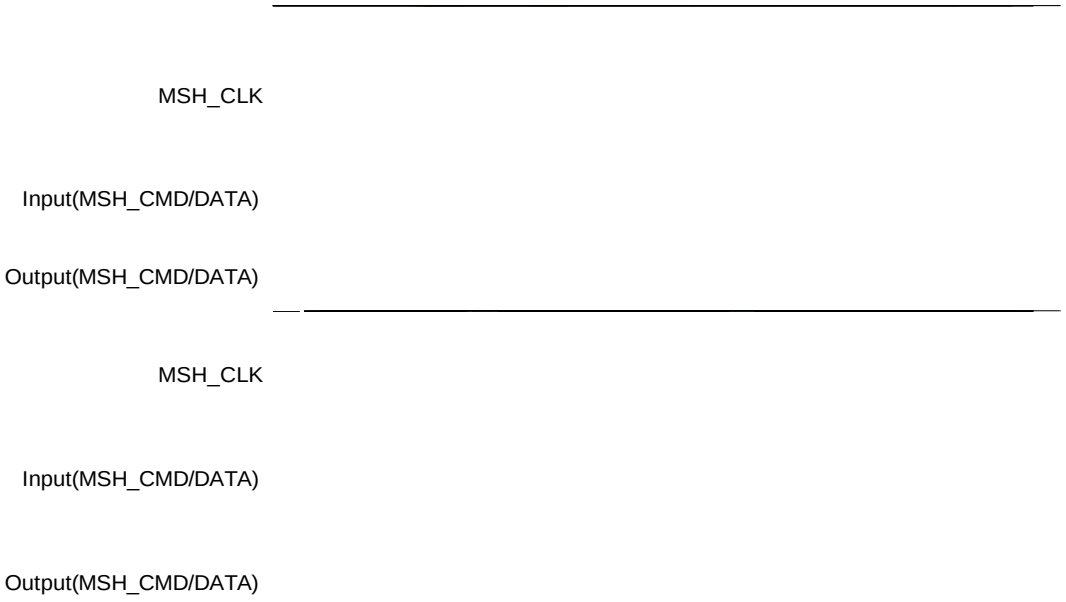

Figure 10-9 : eMMC Interface Timing diagram

10.12 DDR3/DDR4 Timing Parameter

Table 10-16 : DDR4 Interface Timing Parameters

Parameter	Symbol	DDR4-1600		
		Min	Typ	Max
Output clock timing spec				
Average clock period	tCK	-	1.25	-
Average high-pulse width	tCH	0.48	0.5	0.52
Average low-pulse width	tCL	0.48	0.5	0.52
Clock-period jitter	tJIT	-0.063	-	0.063
Output signals timing spec				
Address , command and Bank address setup time to clk	tIS	0.215	-	-
Address , command and Bank address hold time to clk	tIH	0.215	-	-
DQS_P differential high-pulse width	tDQSH	0.46	-	0.54
DQS_P differential low-pulse width	tDQSL	0.46	-	0.54

DQS_P/N falling to CLK_P/N rising	tDSS	0.18	-	-
CLK_P/N rising to DQS_P/N falling	tDSH	0.18	-	-
Input signals timing spec				
DQS_P/N to DQ skew	tDQSQ	-	-	0.16
DQS_P/N differential input high pulse width	tQSH	0.4	-	-
DQS_P/N differential input low pulse width	tQSL	0.4	-	-

Table 10-17 : DDR3 Interface Timing Parameters

Parameter	Symbol	DDR3-800			DDR3-1600			Unit
		Min	Typ	Max	Min	Typ	Max	
Output clock timing spec								
Average clock period	tCK	-	2.5	-	-	1.25	-	ns
Average high-pulse width	tCH	0.47	0.50	0.53	0.47	0.50	0.53	tCK
Average low-pulse width	tCL	0.47	0.50	0.53	0.47	0.50	0.53	
Clock-period jitter	tJIT	-0.10	-	0.10	-0.07	-	0.07	ns
Output signals timing spec								
Address , command and Bank address setup time to clk	tIS	0.200	-	-	0.045	-	-	ns
Address , command and Bank address setup time to clk	tIH	0.275	-	-	0.120	-	-	
DQS_P differential high-pulse width	tDQSH	0.45	-	0.55	0.45	-	0.55	tCK
DQS_P differential low-pulse width	tDQSL	0.45	-	0.55	0.45	-	0.55	
DQS_P/N falling to CLK_P/N rising	tDSS	0.2	-	-	0.18	-	-	
CLK_P/N rising to DQS_P/N falling	tDSH	0.2	-	-	0.18	-	-	
Input signals timing spec								
DQS_P/N to DQ skew	tDQSQ	-	-	0.200	-	-	0.100	ns
DQS_P/N differential input high pulse width	tQSH	0.38	-	-	0.4	-	-	tCK
DQS_P/N differential input low pulse width	tQSL	0.38	-	-	0.4	-	-	

10.13 Trace Signals Timing Parameter

Table 10-18 : Trace Interface Timing Parameters

Symbol	Signals	Description	Min	Max	Units
F_{TRACE}	TRACE_CLK	TRACE clock frequency	-	150	MHz
DC_{TRACE}	TRACE_CLK	TRACE clock duty cycle	TBD	TBD	%
T_{OSU}	TRACE_DATA* TRACE_CTL	TRACE output Setup time	TBD	-	nS
T_{OH}	TRACE_DATA* TRACE_CTL	TRACE output Hold time	TBD	-	nS

11 Thermal Specifications

11.1 Thermal Specification

Thermal specifications for this device are based on the JEDC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specification are modeled using an eight-layer test board with four signal layers, two power planes, and four ground planes (4s6p PCB).

Tj = Ta + θja x Power

Where θja =(θjc || θjb) + θca

θja = Junction to Ambient thermal resistance (°C/W)

θjc = Junction to Package Case thermal resistance (°C/W), Case temperature measured at the top center of the outside surface of the component package

θjb=JunctiontoBoardthermalresistance(°C/W).Boardtemperaturemeasuredatthecenter ball or column location on the outer most ball or column row of the longest side of the package.

θca = Package Case to Ambient thermal resistance (°C/W)

The typical θja is 0.5C/W with heat sink and environment as below:

- Heatsink Widthinmm----------->80
- Heatsink Lengthinmm----------->80
- Heatsink Heightinmm----------->25
- Air FlowinLFPM----------->400
- Heat sink Base Thicknessin mm----------->4
- Heat sink Fins Pitch inmm----------->2.7
- Heat sink Fin Thicknessinmm----------->1
- NumberofFins----------->30
- Thermal Resistance of Heat sinkinC/W----------->0.37 @ 400 LFPM airflow
- Estimated Mass(weight) of Heat sinkingrams----------->233g
- HeatsinkMaterial----------->Extrusion GradeAluminum

Air Flow in LFPM	0	100	200	300	400	600	700
θja (C/W)	2.14	1.68	1.30	1.10	0.97	0.83	0.78
θsa (C/W)	1.80	1.33	0.94	0.73	0.59	0.44	0.39

- Note: θsa is the thermal resistance of proposed heatsink.

- For this package/Diecombination:
- θjc = 0.32 DegreeC/Watt
- θjb = 0.81 DegreeC/Watt

NOTE

- 1. This proposed heat sink solution is a traditional extruded heat sink solution, which meets thermal requirement for a listed application and environmentconditions.
- 2. Note that many more other thermal solutions can be possible for this package and application environments.
- 3. The heat sink attaches process uses phase change material with 3.8 W/m-Kthermal conductivity, 5mil thickness and at least 80% coverage.
- 4. If any of these application conditions or thermal parameters changes, thethermal solution may not work.

11.2 ReflowProfile

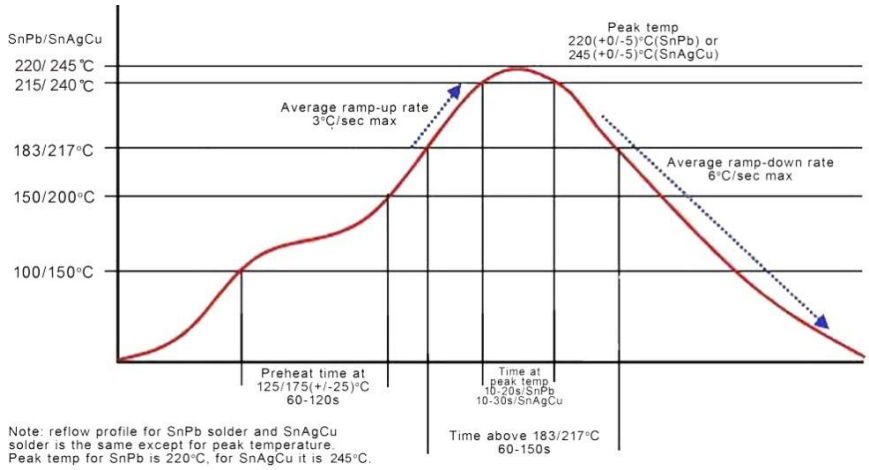

Figure 11-1 5VT6126 Reflow Profile

12 Package Mechanical Dimensions

12.1 Package Description

Table 12-1 is the package size description of 5VT6126

Table 12-1 : Package Mechanical Size

Package Type	Package	Package Dimension	Lead frame	Package thickness(mm) Include BALL	Pin pitch (mm)
FC-PBGA	1143, FC-PBGA	31.0mm*31.0mm	OPL Forced, Lead Free	Nom = 2.656 Max = 2.906	0.800

12.2 Marking

5VT6126 Marking

The descriptions of marking are listed as below:

Marking	Description
“XXXXXX.XXABCD” :	Lot Number
“YYWW” :	Date Code
“R001”:	Revision Level and Number
“ZZ”	Industry Code. “S” means particular industry; any other character including blank means the other industries.

Marking	Description
●	A01 Corner Identifier

12.3 Package Dimension

Figure 12-2, Figure 12-3, Figure 12-4 is the 5VT6126 package mechanical diagram.

TOP VIEW

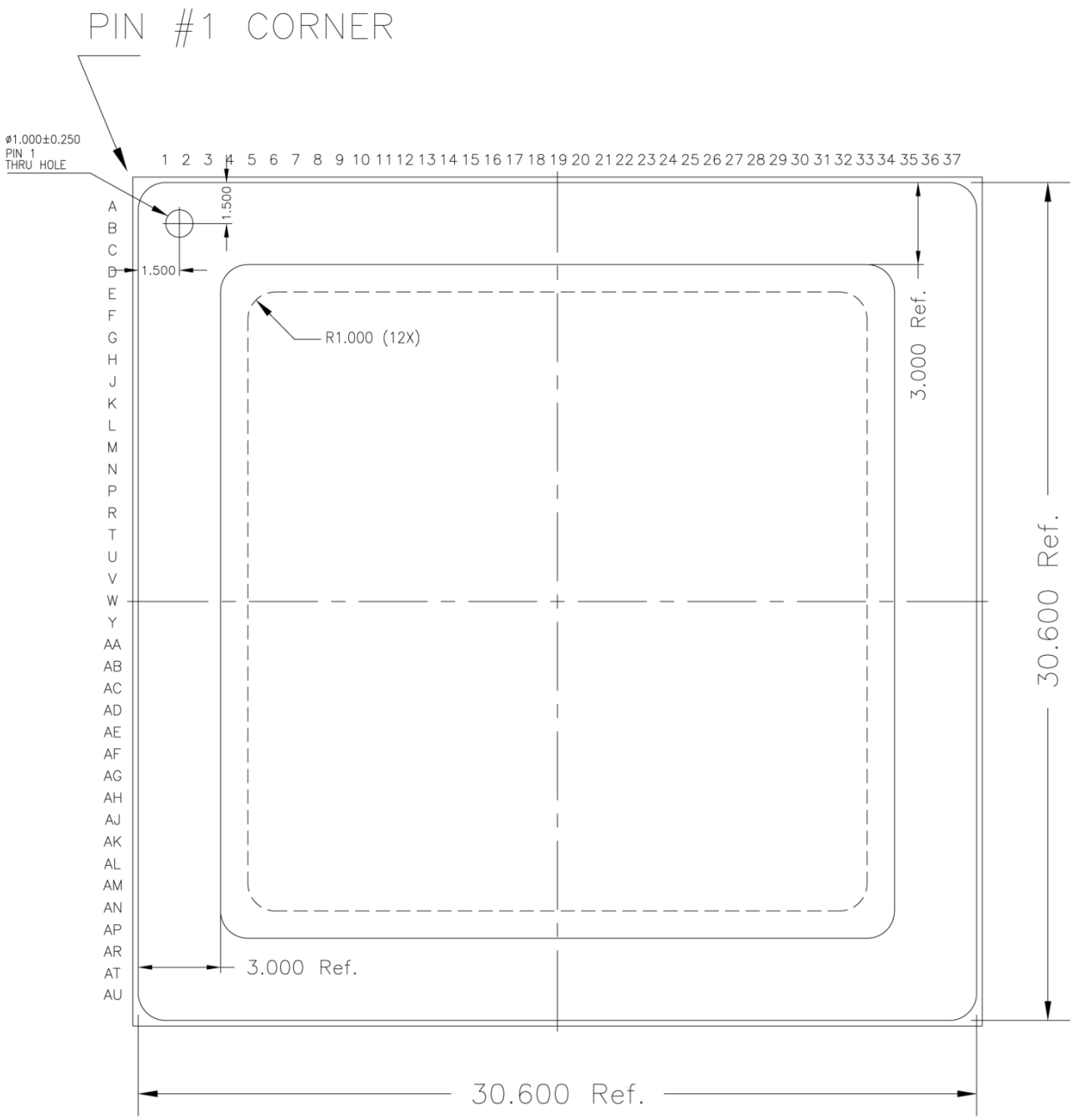

Figure 12-2 : Top view

BOTTOM VIEW

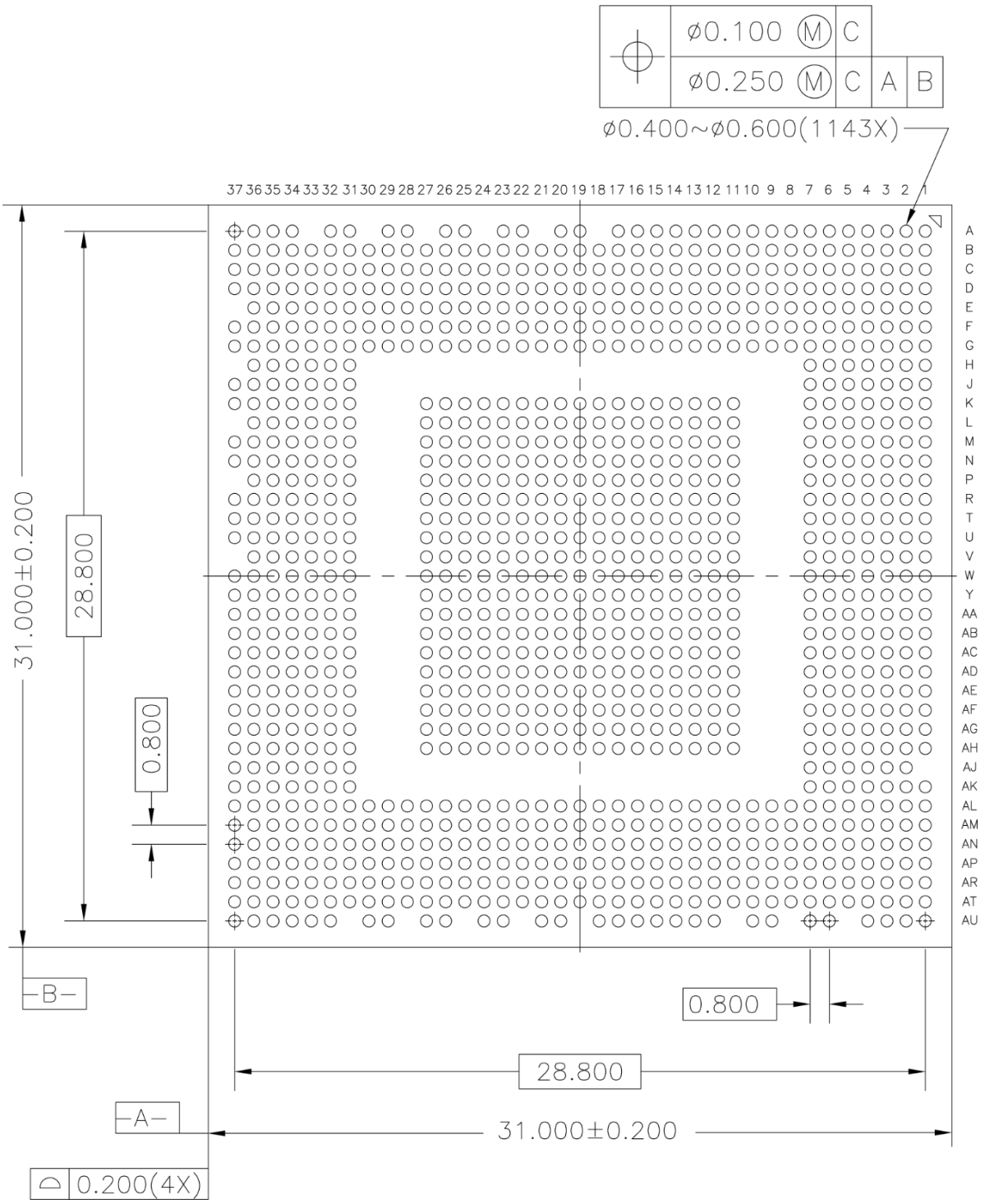

Figure 12-3 : Bottom View

SIDE VIEW

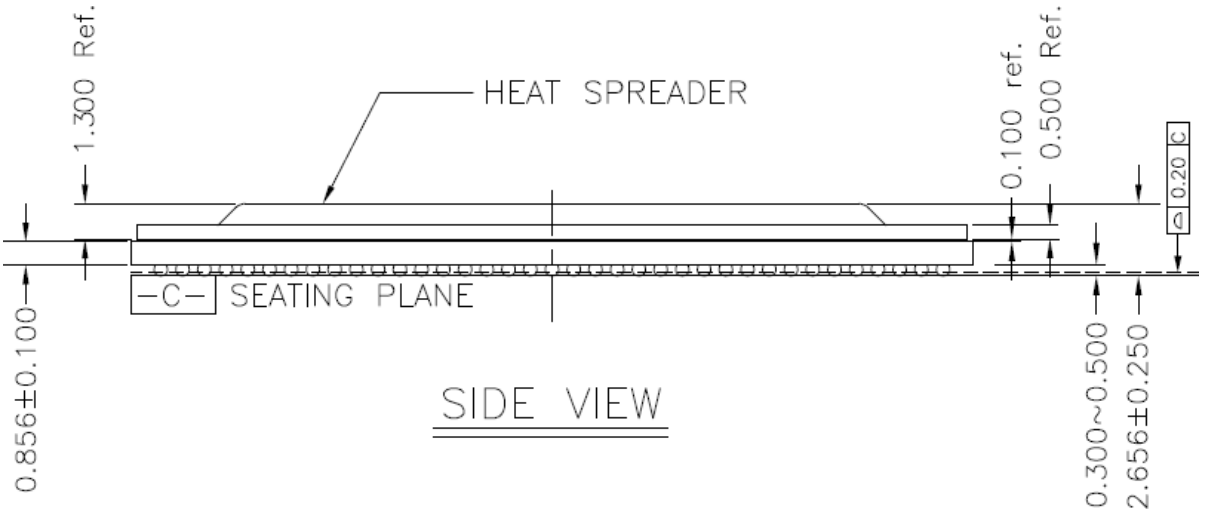

Figure 12-4 : Side View

NOTE

All dimensions are in millimeters.

